

**A NOVEL ANALOG DECISION-FEEDBACK EQUALIZER IN
CMOS FOR SERIAL 10-GB/SEC DATA TRANSMISSION
SYSTEMS**

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Presented to
The Academic Faculty

by

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Doctor of Philosophy

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To My Family

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LIST OF SYMBOLS AND ABBREVIATIONS

ADC	Analog-digital converter
ADFE	Analog decision-feedback equalizer
ALA	Analog limiting amplifier
BER	Bit-error ratio
BERt	Bit-error-ratio tester
CD	Chromatic dispersion
CDR	Clock-data recovery
CID	Consecutive identical digits
CML	Current-mode logic
CMOS	Complementary-metal-oxide semiconductor
CPU	Central processing unit
DAC	Digital-analog converter
DCD	Duty-cycle distortion
DCF	Dispersion compensating fibres
DFE	Decision-feedback equalizer
DJ	Deterministic jitter
DMD	Differential modal delay
DWDM	Dense-wavelength-division-multiplexing
EDC	Electronic dispersion compensator
EMI	Electro-magnetic interference

FBT	Feedback taps
FDDI	Fibre-distributed data interface
FFE	Feed-forward equalizer
FFT	Feed-forward taps
FIR	Finite impulse response
FR-4	Flame-resistant-4
GBW	Gain-bandwidth
HBT	Heterojunction bipolar transistor
IC	Integrate circuit
ISI	Inter-symbol interference
LAN	Local area network
LD	Laser diode
LE	Linear equalizer
LED	Light emitting diode
LLC	Loop latency control
LMS	Least-mean square
MAN	Metropolitan area network
MLSE	Maximum-likelihood-sequence estimation
MMF	Multi-mode fibre
MMSE	Minimum mean-square error
MZM	Mach-Zehnder modulator
NMOS	N-type metal-oxide semiconductor

NRZ	Non-return to zero
PAM	Pulse-amplitude modulation
PCB	Printed circuit board
PDF	Probability distribution function
PLL	Phase-locked loop
PMOS	P-type metal-oxide semiconductor
PMD	Polarization-mode dispersion
PRBS	Pseudo-random bit sequence
PSD	Power spectral density
RJ	Random jitter
SDC	Single-differential converter
SMF	Single-mode fibre
SNR	Signal-noise ratio
TCU	Tap control unit
UTP	Unshielded twisted pair
UI	Unit interval
VCSEL	Vertical cavity surface emitting laser
VGA	Variable gain amplifier
WAN	Wide area network
WDM	Wavelength division multiplexing
ZF	Zero-forcing

SUMMARY

This dissertation develops an unclocked receiver analog decision-feedback equalizer (ADFE) circuit architecture and topology and implements the circuit in 0.18- μm CMOS to enable 10-Gb/sec serial baseband data transmission over FR-4 backplane and optical fibre. The ADFE overcomes the first feedback-loop latency challenge of traditional digital and mixed-signal DFEs by separating data re-timing from equalization and also eliminates the need for clock-recovery prior to decision-feedback equalization.

The ADFE enables 10-Gb/sec decision-feedback equalization using a 0.18- μm CMOS process, the first to do so to the author's knowledge. A tuneable current-mode-logic (CML) feedback-loop is designed to enable first post-cursor cancellation for a range of data-rates and to have external control over loop latency over variations in process, voltage and temperature. CML design techniques are used to minimize current consumption and achieve the required voltage swing for decision-feedback to take place. The all-analog equalizer consumes less power and area than comparable state-of-the-art DFEs.

The ADFE is used to compensate inter-symbol interference (ISI) for 20 inches of FR-4 backplane and 300 m of multi-mode fibre at 10-Gb/sec. The ADFE also extends the reach of single-mode fibre at 10-Gb/sec to 120 km. The work described in this dissertation advances the state-of-the-art in equalization solutions for multi-Gb/sec serial data transmission and can find

applications in several of the 10-Gb/sec Ethernet standards that have been approved recently. The contributions of this work toward future research are also discussed.

CHAPTER 1

INTRODUCTION

1.1 Speed Drivers in Data Transmission Systems

The demand for higher data rates through data transmission systems is always increasing. The growth of the Internet is one of the key factors driving data rates. The basic human demand for communication, as well as acquiring and sharing information over the Internet, is fuelling the demand for software and applications that enable people to perform these activities quickly, which in turn is fuelling the demand for higher computer processing and data transmission speeds.

In addition, advances in central processing unit (CPU) architecture like multiple cores per CPU and multi-threads per core, as well as improvements in silicon process speeds, have pushed CPU performance to billions of instructions per second. However, CPU speed is of little significance if limitations in the physical media for chip-to-chip, board-to-board, server-to-server and local-area network (LAN)-to-LAN connections keep the total processor-to-network throughput low. The theoretical maximum capacity of optical fibre is also driving data rates over other types of media higher as network providers attempt to take full advantage of the massive capacity of optical fibres as a transmission medium. Network data rates are limited by channel noise, non-ideal dispersion effects in optical fibres and bandwidth limitations in copper channels, as well as by the speed limitations of the electronics in a data transmission system. In brief, demand

for high bandwidth applications, advances in CPU processing speed, as well as advances in optical fibre and related technologies, are the key accelerators for higher data rates in data transmission systems.

1.2 The Challenge for 10-Gb/sec Data Transmission

The Internet consists of a large number of interconnected networks comprising of individual users connected to servers, servers connected to LANs and LANs connected together to form metropolitan area networks (MANs). A wide area network (WAN) is comprised of LANs and MANs. The advent of using optical fibre for data transmission in the late 1960's enabled much higher data rates to be transmitted through networks than through copper coaxial cable due to the inherent capacity of light as a transmission medium [1.1]. Further advancements in fibre optics such as dense wavelength division multiplexing (DWDM), which multiplexes several signals onto a single fibre using different wavelengths, and the development of high-speed tuneable lasers, optical splitters and other optical components have further increased the capacity of optical networks [1.1]. However, long-haul DWDM systems and optical transceivers are expensive to install and maintain and not economical if the full network capacity is not used. Therefore, fibre was traditionally used only for long-haul WAN backbone links (>100 km). However, as data rates increased, fibre moved to the MAN and enterprise LAN backbones as well. Since multi-mode fibre (MMF) enables the use of lower-cost transceivers and connectors, MMF has dominated in shorter-reach LAN applications. Single-mode fibre (SMF), which can support higher data-rates than MMF, but requires more expensive connectors and transceivers, has been used in longer-reach MAN and WAN

applications. Much of the last-mile connectivity and connectivity within data centres and servers continues to be on copper-based electrical channels like unshielded twisted-pair (UTP), coaxial cable and FR-4 backplane. As data rates increase to 10-Gb/sec, installed MMF, backplane, coaxial cable and UTP are the primary speed bottlenecks within enterprise network and data centres, in blade server chassis, and in core LAN/MAN Ethernet switches and routers.

Over the years, several data transmission standards, namely, Ethernet, Infiniband, Fibre Channel, and PCI Express have been developed for different applications. The standards are constantly being upgraded to specify higher data rates that meet the growing demand for network speed. For example, the first Ethernet standard specified data rates of 10-Mb/sec and then advanced to 100-Mb/sec and 1-Gb/sec. 10-Gb/sec is the next frontier for Ethernet. Standards for 10-Gb/sec Infiniband and 10-Gb/sec Fibre Channel have also been approved. The potential applications for serial 10-Gb/sec data transmission systems is substantial; from very-short reach applications (<1 m) on a backplane in a server chassis, to short reach applications such as connecting switches within a data centre over coaxial cable (<15 m); to medium-reach applications such as connecting the data centre to the wiring closet in enterprise LANs using MMF (< 300m); to long reach applications such as connecting buildings in a university campus or a multi-site company using SMF [1.2] as well as for very-long reach applications such as MAN and WAN connectivity over SMF. Figure 1.1 shows a diagram of the potential application space for 10-Gb/sec. Furthermore, several key components for 10-Gb/sec data transmission systems, such as 10-Gb/sec lasers and laser drivers are already commercially available.

Foreseeing the demand, a number of standards for 10-Gb/sec data transmission have been approved varying by application and specifications. As of 2007, the IEEE 802.3ae for 10 Gigabit Ethernet over single-and multi-mode fibre, the IEEE 802.3ak for 10 Gigabit Ethernet over twin-axial cable, the IEEE 802.3an for 10 Gigabit Ethernet over twisted-pair copper-cabling, the IEEE 802.3ap for 10 Gigabit Ethernet over FR-4 backplane and the IEEE 802.3aq for 10 Gigabit Ethernet over multi-mode fibre (MMF) are some of the standards for 10-Gb/sec data transmission that have been approved [1.3]. The next few years will determine which of these standards will gain commercial acceptance among component vendors and network service providers.

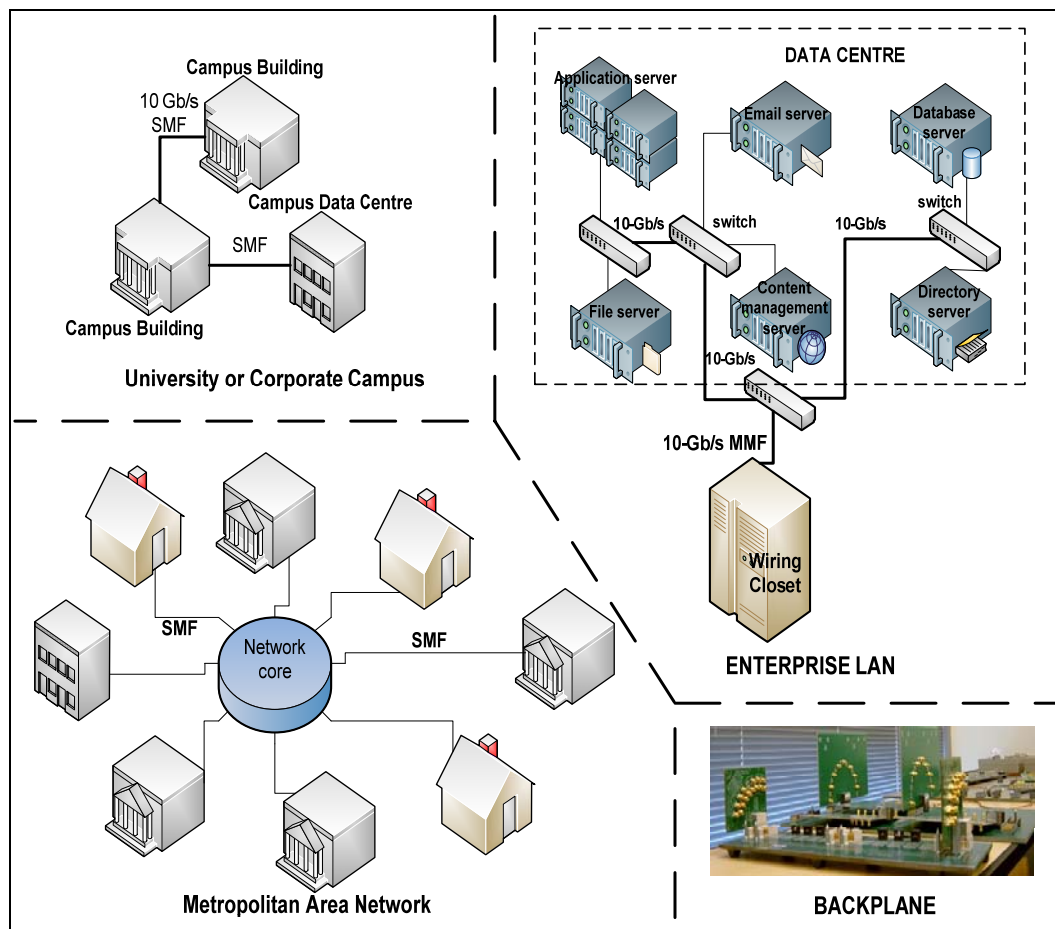


Figure 1.1 Potential areas of application for 10-Gb/sec connectivity.

The challenge arises from the fact that much of the infrastructure installed in commercial data transmission systems was aimed at handling data rates in the Mb/sec range or up to a few Gb/sec. The first IEEE Ethernet standard, adopted in 1981, was the IEEE 802.3 standard for 10-Mb/sec data over coaxial cable [1.3]. Later standards were also defined for transmission over CAT-3, CAT-5 and optical fibre. With the rapid increase of digital multi-media traffic in LANs, as well as in data centres and corporate intranets, new standards for 100-Mb/sec, 1-Gb/sec and 10-Gb/sec Ethernet were adopted [1.3]. With every new standard, the existing networking infrastructure must migrate to handle higher data rates to maintain cost-effectiveness. New technology must be cost-effective in order for businesses and consumers to adopt it. This infrastructure includes single- and multi-mode optical fibre installed for long-haul and short-haul links, coaxial cables for server-to-server connections, or backplanes for line-card-to-line-card and chip-to-chip connections, among others. Due to impairments in signal integrity, which will be discussed in more detail in the following section and chapter, as data rates coming down the system increase, these legacy channels that were installed to support slower data rates act as a bottleneck in the transmission system, significantly increasing the bit-error-ratio (BER) and data loss. Of course, newer cables with more capacity can support the higher data rates. However, the cost of refurbishing the entire infrastructure is prohibitive for most data centre operators and transmission system providers. Businesses prefer seamless transition and re-use of existing technology and infrastructure as much as possible. Therefore, there is an urgent need and a ready market for cost-effective solutions that will enable the migration of existing networking infrastructure to support 10-Gb/sec data rates. This has created an

interesting research area for circuit designers to develop innovative integrated circuit (IC) solutions.

The 10-Gb/sec Ethernet standards that have been defined recently also reflect this demand. For example, the 10GBASE-LRM (IEEE Std. 802.3aq™-2006) standard, targeted toward enterprise LAN applications, is defined for transmission over multi-mode fibre-distributed-data-interface (FDDI) grade fibre that was installed in the early 1990's. The standard specifies using 850 nm wavelength of light and requires 10-Gb/sec transmission over 220 m with a BER < 10^{-12} [1.3]. However, at 10-Gb/sec, FDDI-grade fibre only supports 26 m [1.4]. Despite this, out of all the 10-Gb/sec standards defined for MMF, this one has gained popularity among component vendors because it enables the use of installed fibre, which still comprises a substantial percentage of installed fibre world-wide, enabling a lower cost solution. The 10GBASE-LRM standard specifies the use of electronic dispersion compensation (EDC) ICs to achieve the required transmission reach [1.3].

Similarly, the 10GBASE-KR (IEEE Std. 802.3 ap™-2007) standard specifies 10-Gb/sec data transmission over 1 m of installed FR-4 backplane and specifies adaptive receiver equalization to achieve the required transmission reach [1.3].

1.3 Signal Integrity and Equalization

Maintaining signal integrity is an important requirement in data transmission systems. The signal can be an electrical signal, an optical pulse, or an electromagnetic signal. The core of a communication link consists of a transmitter that generates the signal, a communication channel that carries the signal and a receiver that accepts the signal and processes it correctly.

For accurate communication, it is important that the integrity of the signal is maintained at all points of this transmission. From a physical layer standpoint, this means that if a “1” is sent from the transmitter and down the channel, be it copper, optical fibre or air, the receiver should also determine that the signal is a “1”. This is a fundamental challenge for data transmission system and circuit designers due to the various factors affecting signal integrity.

Signal integrity in data transmission systems is affected by a number of factors. Apart from random noise, atmospheric and man-made noise, there are deterministic factors that contribute to deteriorating signal integrity. Copper-based signal transmission is affected by the limited bandwidth of copper channels and crosstalk from adjacent channels. Optical signals are affected by frequency-independent loss of optical power as they travel down the fibre as well as dispersion-causing mechanisms depending on the type of fibre. Bandwidth limitations in copper and pulse dispersion in optical fibres result in inter-symbol-interference (ISI) at the receiver. Typically, ISI deteriorates as the data rate and the length of the channel increases. ISI is the primary factor limiting transmission distances over copper-based transmission channels and optical fibre at 10-Gb/sec. ISI is also a source of deterministic jitter, which will be discussed in detail in the next chapter. Jitter can significantly increase BER, resulting in data loss. Compensating for ISI and maintaining signal integrity over installed transmission media at 10-Gb/sec is very important to service providers and enterprise network managers and has opened up an exciting field of research for system and circuit designers.

Equalization is a process of conditioning the electrical signal, either at the transmitter or the receiver to compensate for channel-induced ISI and improve signal integrity. Linear and non-linear equalization techniques have been explored in the literature. With advances in semiconductor processes, as well as analog and digital signal processing, equalizer circuits can be implemented in silicon and integrated with the transceiver circuitry, thereby providing a cost-effective solution to the signal integrity problem in data transmission systems. Despite having a lower transition frequency, f_t , than other commercial processes like silicon-germanium (SiGe) and indium-phosphide (InP) heterojunction bipolar transistors (HBTs), complementary metal-oxide semiconductor (CMOS) technology is the process of choice for such high-speed networking ICs because it offers the advantages of low-cost and higher levels of integration compared to other faster processes.

1.4 CMOS Equalizer Design Challenges

When data transmission operating speeds were in the Mb/s range, equalization and other signal processing could be performed using digital CMOS circuits. The improvements in digital CMOS processes enabled all signal processing functions to be integrated on single chip. However, as data rates move beyond 5-Gb/sec, the switching speed of CMOS transistors becomes a critical bottleneck and implementing multi-Gb/sec ICs poses a huge challenge for circuit designers.

For a digital receiver, an analog-digital converter (ADC) operating at the data rate is required at the front-end prior to any other signal processing. Multi-Gb/sec ADCs in standard CMOS are limited by the transistor switching speed and the time taken to regenerate a small analog signal to digital

CMOS voltage levels. To operate at faster speeds, designers have to move to more expensive process nodes with smaller channel lengths. Current 10-Gb/sec ICs are being manufactured at 90 nm CMOS [1.5]. In addition, 65 nm and 45 nm CMOS ICs for data transmission are not far into the future. However, as the channel length decreases, the trade-off for faster switching speeds is increased static and dynamic power dissipation, reduced voltage headroom, increased leakage current, IR drop and switching noise [1.6], [1.7]. For these reasons, analog signal processing has gained momentum in the field of multi-Gb/sec transceivers for data transmission. Analog circuits can provide increased bandwidth compared to digital circuits on the same process node. By delaying the analog-to-digital conversion further down the receiver chain, the designer can perform as many signal processing functions in the analog domain, potentially reducing area and power consumption. This thesis demonstrates a 10-Gb/sec analog decision-feedback equalizer (DFE) in 0.18- μm CMOS. Comparable digital DFE circuits utilize 90 nm CMOS to achieve 10-Gb/sec operation.

1.5 Organization

The dissertation will be organized as follows:

Chapter 2 begins with a study of key concepts in baseband data transmission systems and an introduction to inter-symbol interference (ISI) in backplanes and optical fibres. The concept of equalization to compensate for ISI is introduced and various equalizer schemes are looked at. Linear feed-forward equalization and its limitations are explained. Non-linear equalization techniques such as decision-feedback equalization and maximum-likelihood sequence estimation (MLSE) are described. Chapter 3

studies the limitations imposed by CMOS process on conventional digital circuit architectures and introduces some high-speed analog circuit techniques and topologies that can replace traditional digital circuit topologies. The traditional DFE and the challenges of implementing the DFE in standard CMOS at multi-Gb/sec data rates are explained. State-of-the art implementations and techniques in the open literature are looked at. Chapter 4 introduces the analog DFE (ADFE). The building blocks, circuit architecture and relevant simulation results are shown. The circuits are implemented in TSMCs 0.18- μm mixed-mode CMOS process. High-speed layout techniques are utilized to minimize layout parasitic elements and achieve faster data rates. Chapter 5 presents the measurement results. Chapter 6 concludes with a summary of the key technical achievements and suggestions for future work.

CHAPTER 2

SIGNAL INTEGRITY AND EQUALIZATION

This chapter introduces the problem of signal integrity in wired baseband data transmission systems and equalization ICs as a possible solution. In particular, the chapter looks at baseband channels, such as the backplane channel, as well as optical fibre channels that transmit baseband data using light as the carrier frequency. Section 2.1 defines some key terms and concepts that are used in later sections of the dissertation. In particular, this section introduces the concepts of pulse-amplitude modulation (PAM), pseudo-random bit sequences (PRBS), differential signalling and jitter. Section 2.2 focuses on data transmission through bandwidth limited baseband channels, with emphasis on the backplane channel, and the resulting inter-symbol-interference (ISI). Section 2.3 looks at the problem of optical pulse dispersion in multi-mode and single-mode optical fibre and the resulting ISI that is seen after opto-electric conversion. ISI is identified as a limiting factor in legacy backplanes and installed optical fibre at 10-Gb/sec data rates. Section 2.4 introduces equalization as a technique to compensate for ISI and improve signal integrity in backplanes and optical fibres. Pre-and post-cursor ISI are defined and important equalization techniques are introduced and analyzed with the aid of system simulations. Section 2.5 introduces the decision-feedback equalizer (DFE).

2.1 Baseband Digital Transmission Systems

The transmission of digital information over electric transmission channels, such as copper cables, is called baseband transmission because it does not involve the use of a carrier signal as in wireless data transmission. Strictly speaking, a channel is called a baseband channel if the frequency passband of the channel includes zero frequency, $f = 0$. This is in contrast to a wireless transmission channel which is a bandpass channel. In wireless data transmission, the information to be transmitted modulates a carrier frequency, which shifts the frequency content of the information signal to the appropriate frequency band [2.1]. The data being transmitted is also called baseband data since it is at its original frequency and not impressed upon a carrier. Most wired channels such as coaxial cable, unshielded twisted-pair cable, and FR-4 backplane are examples of baseband channels. Although digital baseband transmission systems involve the transmission of digital data or bits, the baseband channel itself is analog, susceptible to Gaussian noise and other interference, and the digital information sequence to be transmitted is mapped onto a continuous-time analog waveform using some type of modulation technique. Since the actual signal being transmitted is an analog waveform, it is affected by the channel through which it is being transmitted. Random noise, crosstalk from signals in adjacent channels, electro-magnetic interference (EMI), and bandwidth limitations of the transmission channel are some of the factors that affect the integrity of the analog waveform. The following sub-sections define some key terms and concepts in baseband digital transmission systems.

2.1.1 Pulse-Amplitude Modulation (PAM)

The digital information to be transmitted is mapped onto a continuous-time electrical signal using some sort of modulation technique. Pulse-amplitude modulation (PAM) is the simplest and most commonly used digital modulation technique in baseband transmission systems. In binary non-return-to-zero (NRZ) PAM, as shown in Figure 2.1(a), a bit 1 is represented as a pulse of amplitude A and a bit 0 is represented as a pulse of amplitude $-A$. R_b is the bit rate and T_b is the bit duration.

$$R_b = \frac{1}{T_b} \quad (2.1)$$

M-ary PAM is a generalization of binary PAM, where each symbol is composed of k bits and M signal amplitude levels.

$$M = 2^k \quad (2.2)$$

Therefore, a 4-PAM signal, as shown in Figure 2.1(b), has 4 possible signal levels and each level represents a symbol. Each symbol is mapped to two bits. In this case, the symbol rate is R_s and the symbol period is T_s .

$$R_b = 2R_s \quad (2.3)$$

For a 2-PAM signal, $R_b = R_s$. Therefore, assuming equal symbol rate, a 4-PAM signal has twice the data throughput of a 2-PAM signal. Since the symbol rate determines the signal bandwidth, 4-PAM has double the spectral efficiency of 2-PAM. However, assuming equal transmitted power, 2-PAM has better SNR than 4-PAM because the signal levels are spaced farther apart [2.2]. In other words, a 4-PAM signal requires twice the transmitted power to achieve the same SNR as a 2-PAM signal [2.2].

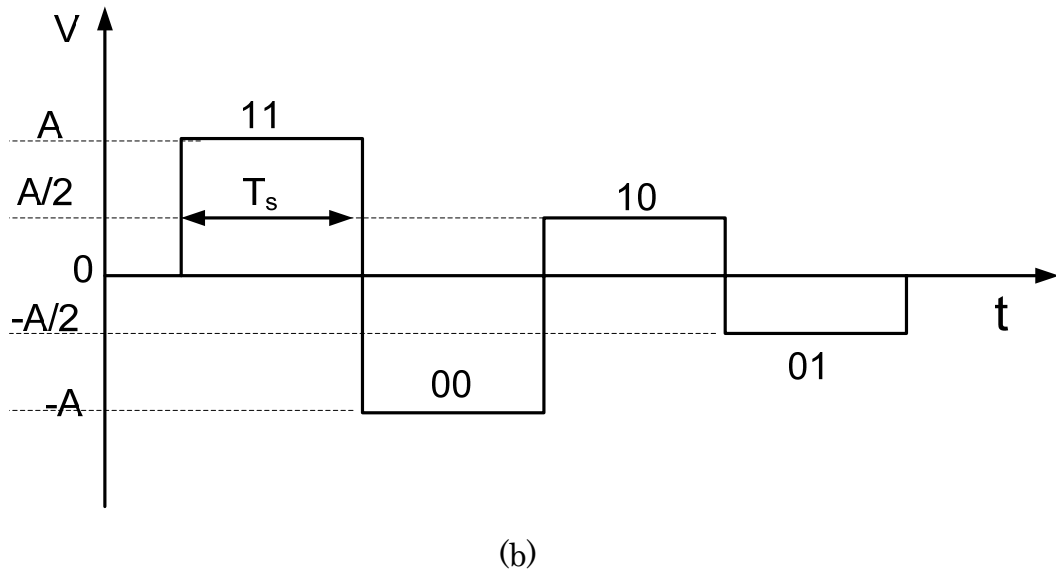
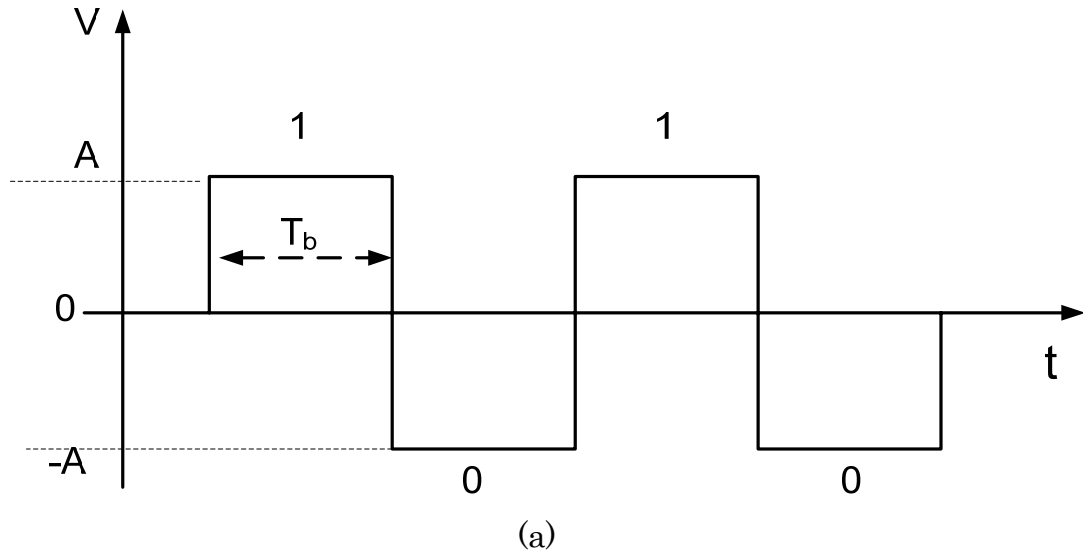


Figure 2.1 (a) 2-PAM signal and (b) 4-PAM signal.

2.1.2 Power Spectral Density of NRZ PAM

A NRZ PAM data pattern has a power spectral density (PSD), which shows the spectral content of the time-domain signal. In simple words, the PSD is the *bandwidth* of the time-domain signal. The PSD is dependent on the type of PAM, the pattern of 1's and 0's and the coding utilized. Since the

data has to travel through band-limited channels, system designers try to decrease the spectral content or bandwidth of the transmitted NRZ data pattern. The PSD of a NRZ test pattern, as defined by (2.4), is obtained by computing the Fourier transform of the autocorrelation function of the test pattern [2.3].

$$S_y(\omega) = T_b \text{sinc}^2\left(\frac{\omega T_b}{2}\right) \quad (2.4)$$

2.1.3 Pseudo-Random Bit Sequence (PRBS) Basics

A pseudorandom bit stream (PRBS) pattern is a general purpose test pattern used in encoded, random, and scrambled NRZ applications. It provides a good representation of scrambled random NRZ data that is experienced in “real-world” applications. A PRBS pattern is defined as $2^x - 1$, where x is the length of the shift register used to create the pattern. The pattern length is $2^x - 1$. Each $2^x - 1$ PRBS contains every possible combination of x bits (except one). x also denotes the maximum number of consecutive identical digits (CIDs) in a PRBS pattern [2.3]. The PSD of a PRBS pattern is a series of discrete spectral lines scaled by a $\text{sinc}^2(f)$ envelope, where $\text{sinc}^2(f)$ is defined by (2.5).

$$\text{sinc}^2(f) = \frac{\sin f}{f} \quad (2.5)$$

The nulls in the $\text{sinc}^2(f)$ envelope occur at multiples of the bit rate R_b . The discrete spectral lines are spaced at $1/L$, where L is the pattern length in units of time and defined by (2.7).

$$T_b = \frac{1}{R_b} \quad (2.6)$$

$$L = (2^x - 1)T_b \quad (2.7)$$

The magnitude of the $\text{sinc}^2(f)$ function decreases as the data rate and/or the pattern length increases. Figure 2.2 shows the PSD of a PRBS 2^7-1 pattern at 10-Gb/sec. Knowledge of the test pattern PSD is important in order to design the receiver. The bandwidth of the receiver should be large enough to receive the critical components of the test pattern and not so large as to admit excessive noise.

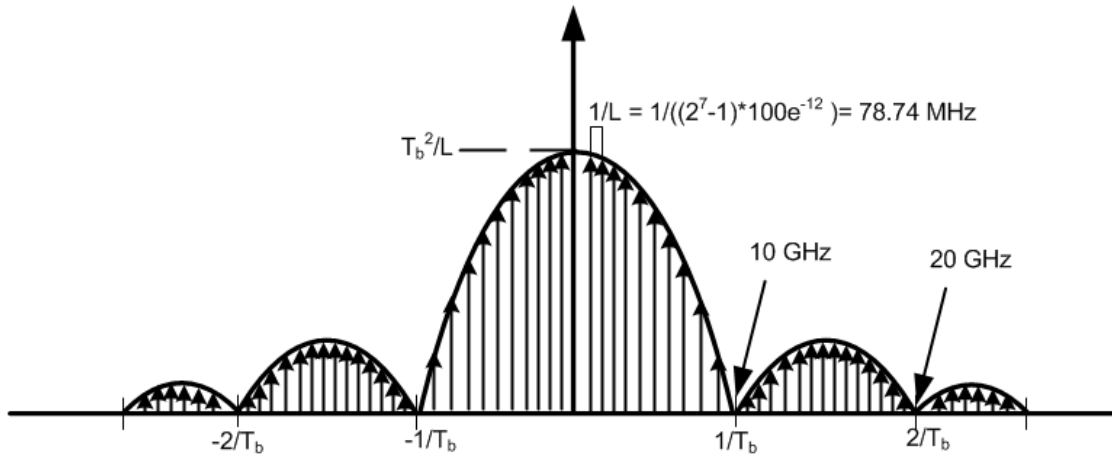
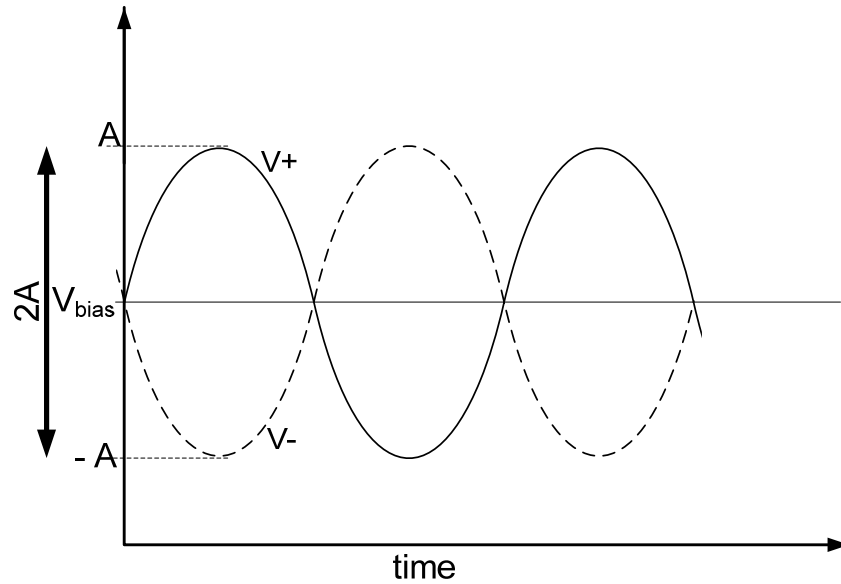


Figure 2.2 PSD of 10-Gb/sec PRBS 2^7-1 NRZ data.

2.1.4 Differential Signalling

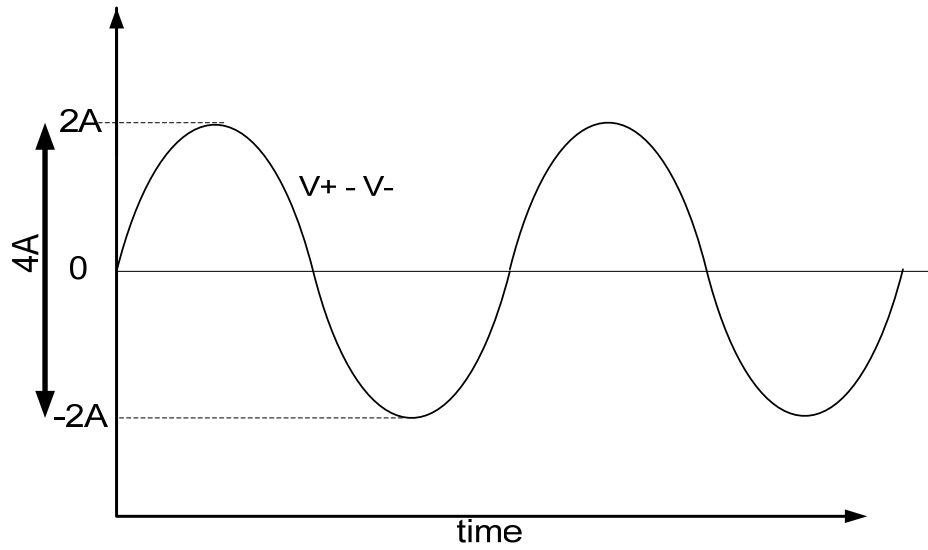
In differential signalling, the information is transmitted using two complementary signals, V^+ and V^- , over two separate channels or wires. The signal value is the difference of the two complementary signals as shown in Figure 2.3. V_{bias} is defined as the ‘common mode’ of the signal. Differential signalling is used extensively in high-speed data transmission systems where signal integrity is critical. Most high-speed circuits and systems use differential signalling to take advantage of the benefits of better noise and

electro-magnetic interference (EMI) immunity, twice the dynamic range for a given signal swing, and the ability to process bipolar signals in a single-supply system without the need of a virtual ground [2.4]. Many transmission systems such as backplane, USB, Firewire, and most Ethernet physical layers use differential signalling. The transmission through optical fibre is single-ended. However, a single-to-differential-converter (SDC) circuit after the photodetector can convert a single-ended signal to a differential signal for further processing in the receiver. Many modern commercial photodetectors have in-built SDCs to provide the receiver with a differential input signal.



(a)

Figure 2.3 (a) Differential signals (b) Single-ended representation.



(b)

Figure 2.3 continued.

2.1.5 Jitter

Jitter is a significant factor affecting signal integrity in multi-Gb/sec baseband data transmission systems. Jitter can be defined as the variation in the transition point of the signal. As data rates increase, jitter can become a significant problem and cause transmission errors in baseband data transmission systems. Jitter also makes clock recovery a challenge when edge detection is being used to recover the system clock from the received data stream. Figure 2.4 shows an eye-diagram with jitter. The optimum sampling point is at the centre of the eye. The bit period, T is equal to the unit interval time, t_{UI} . As the amount of jitter, t_{TJ} , increases, the eye-opening, $t_{eye-width}$ decreases. If the jitter increases up to the centre of the eye, the sampler could make an error in determining the bit value resulting in an error. The eye-width is sometimes expressed as a percentage of the unit interval. It is clear to see that as jitter increases, the percentage value decreases.

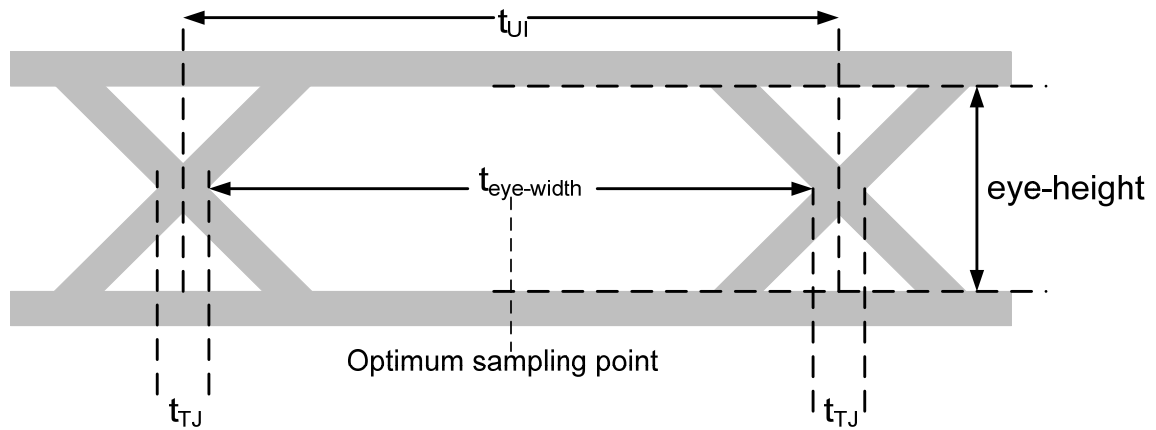


Figure 2.4 Eye-diagram with jitter.

Jitter can be quantified as follows [2.5]:

1. Cycle-To-Cycle Jitter: The time difference between successive periods of a signal.
2. Period Jitter: An RMS calculation of the difference of each period from a waveform average.
3. Time-Interval Jitter: The difference in time between the actual threshold crossing and the expected transition point.

Jitter is usually classified into two types depending on the source of the jitter; random and deterministic. Random jitter (RJ) is not bounded and can be described by a Gaussian probability distribution function (PDF). It is characterized by its standard deviation (rms) value and results from random noise sources such as:

1. Thermal noise, which is related to electron flow in semiconductors and increases with temperature, bandwidth and noise resistance.

2. Shot noise, which is electron and hole noise in semiconductors that depends on bias current and measurement bandwidth.
3. Pink or 1/f noise [2.5].

Deterministic jitter is bounded and described by a non-Gaussian PDF. It is characterized by its bounded peak-to-peak value and can be system-dependent or data-dependent. System-dependent jitter sources include radiation from EM sources, crosstalk, and power supply switching noise. Data-dependent jitter is caused by:

1. Inter-symbol Interference (ISI).
2. Duty-cycle distortion (DCD).
3. Pseudo-random bit sequence (PRBS) pattern.
4. Sinusoidal or periodic jitter related to the data pattern.

The total jitter (TJ) is usually defined as:

$$TJ = DJ + n * RJ \quad (2.8)$$

n depends on the BER specified for the system [2.6]. It is important for circuit and system designers to understand the sources of jitter so that they can find ways to minimize it. Most data transmission receivers have a clock-and-data recovery (CDR) circuit that samples the received data and recovers the system clock using a phase-locked-loop (PLL). The system clock is needed by all the digital blocks in the receiver. Excess jitter in the received signal can make clock recovery very challenging for CDR circuit designers. Jitter reduction and clock recovery poses a significant challenge for multi-Gb/sec receiver designers. Equalization prior to clock recovery can significantly reduce the jitter and relax the requirements of the CDR. Equalization is a process of cancelling ISI and thereby reducing data-dependent jitter.

2.2 NRZ Transmission through Baseband Channels

NRZ data transmission through baseband channels is limited by the bandwidth limitations of the channel. Bandwidth limitations result in inter-symbol interference (ISI) at the receiver. Excessive ISI can result in a complete closing of the eye-diagram and make data recovery impossible. In bandwidth limited legacy baseband channels, ISI is the key factor limiting transmission distances at 10-Gb/sec. ISI is also a key component of deterministic jitter that further impairs signal integrity [2.5, 2.6]. ISI also reduces tolerance to noise.

2.2.1 Nyquist Criterion

We can understand the phenomenon of bandwidth limitations in baseband data transmission and the resulting ISI from a frequency domain perspective. Theoretically, an ideal baseband signal, which is a train of rectangular pulses, has infinite bandwidth. However, the essential bandwidth is finite as shown in Section 2.1.3. For example, most of the power of a 10-Gb/sec PAM signal is contained within the essential band of 0 to 10 GHz, which is the location of the first null in the PSD. On a spectrum analyzer, the spectrum of a NRZ PAM signal consists of frequencies from DC up to the bandwidth of the spectrum analyzer. However, any baseband transmission channel has a finite bandwidth, which can be called W . If W is less than the essential bandwidth of the signal, while a majority of the signal power is transmitted, some portion of the signal spectrum is suppressed. As we know from basic signal processing theory, spectral distortion results in a

spreading of signal energy in the time domain [2.7]. (2.9) represents this phenomenon using the Fourier transform notation.

$$\frac{1}{|a|} F\left(\frac{\omega}{a}\right) \leftrightarrow f(at) \quad (2.9)$$

A square pulse at the input of such a channel is dispersed at the output of the channel, since the low-pass frequency characteristic of the channel causes a smoothening of the sharp rise and fall edges of the square pulse. As shown in Figure 2.5, when a pulse train of 1 and 0 symbols is transmitted through such a channel, this smoothening-out effect causes one symbol to spread out into adjacent symbols. This is called inter-symbol interference (ISI). In short, ISI is caused by limitations in the channel bandwidth and the resulting distortion of the signal spectrum. The Nyquist criterion for ISI-free transmission is that the system bandwidth $W > R_s/2$, where R_s is the symbol rate [2.7]. This is the theoretical minimum system bandwidth required for ISI-free transmission of symbols at a data rate of R_s . So for 10-Gb/sec NRZ signalling, the Nyquist bandwidth is 5 GHz.

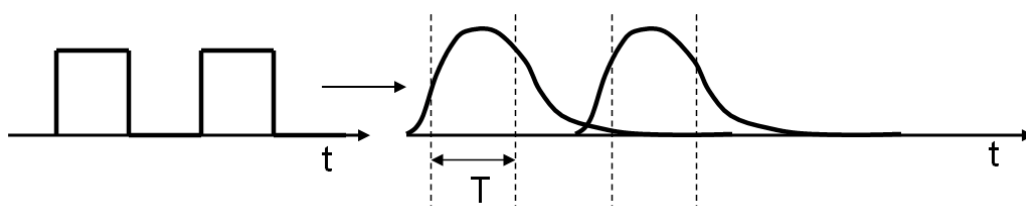


Figure 2.5 Pulse broadening due to attenuation of high frequency signal content.

2.2.2 Backplane Transmission

A legacy backplane is a good example of a baseband channel that is bandwidth-limited and exhibits excessive ISI at 10-Gb/sec. A backplane is a printed circuit board (PCB) used to connect several line cards together. Backplanes are typically found in disk enclosures, disk arrays and servers and are commonly used to connect multiple hard drives to a single controller. As data rates coming down networks increase to 10-Gb/sec, backplanes must also support the increased data rates to maintain overall network throughput. However, attenuation of the high-frequency components of a baseband signal and the resulting ISI results in poor BER through installed backplane systems. The 10GBASE-KR standard for 10-Gb/sec NRZ transmission over FR-4 backplane was approved in 2007 and specifies the need for receiver equalization in order to achieve the required BER [1.3].

A photograph of a backplane with line cards connected by conductive transmission lines is shown in Figure 2.6. The transmitter and receiver integrated circuits (ICs) are on the line cards and use the backplane traces as a transmission medium. The backplane is made of a dielectric material, usually flame-resistant-4 (FR-4). The conductive traces are usually made of copper. The three primary factors that limit data transmission through backplane channels are reflections, crosstalk and loss. Loss due to reflections is minimized by using better impedance controlled connectors, packages and vias. Crosstalk is minimized by using better shielding for connectors, traces and vias. The signal loss through a backplane copper trace consists of conductor loss as well as dielectric loss. At multi-GHz frequencies, dielectric loss dominates conductor loss [2.8].



Figure 2.6 Backplane with line cards and connectors.

Conductor loss consists of DC loss, surface roughness loss, and skin-effect loss. Since the dielectric material is not a perfect insulator, there is a loss at DC associated with current flowing through the dielectric between the signal conductor and the ground plane. Surface-roughness loss is due to the surface roughness of copper and increases with frequency. The skin effect is a physical phenomenon in which an AC current in a conductor distributes itself so that the current density at the surface of the conductor is greater than at its core. Therefore, the current tends to flow at the “skin” of the conductor. The skin effect causes the effective resistance of the conductor to increase with the square root of signal frequency [2.9]. The attenuation due to skin effect increases with increasing effective resistance. The attenuation α is given as,

$$\alpha = \frac{R}{Z_0 W} \quad (2.10)$$

where Z_0 is the characteristic impedance of the conductor and W is the width of the conductor. The effective resistance R is given as,

$$R = \frac{\rho}{d} \quad (2.11)$$

d = skin depth and is given as,

$$d = \sqrt{\frac{2\rho}{\omega\mu_0}} \quad (2.12)$$

ρ = resistivity of conductor

$\omega = 2\pi \times$ frequency

μ_0 = absolute magnetic permeability of the conductor

Therefore,

$$R = \sqrt{\frac{\omega\mu_0\rho}{2}} \quad (2.13)$$

Substituting (2.12) in (2.9), it can be seen that skin effect loss has a $f^{-1/2}$ characteristic. Dielectric loss has a f^{-1} characteristic [2.9]. Beyond 2 GHz dielectric loss dominates skin effect loss in FR-4 channels [2.9].

A backplane trace can form a 2-port network. Figure 2.7 shows the S_{21} or forward transmission of a 20-inch trace of backplane channel. The trace length includes the portion of the trace on the daughter cards. As expected, the traces exhibit a low pass frequency characteristic causing high frequency components to be attenuated more than lower frequency components. The 3-dB bandwidth is much less than the Nyquist frequency of 5 GHz required for 10-Gb/sec data transmission. At 5 GHz the channel has a 20 dB loss. As a result, NRZ data through a 20-inch backplane exhibits excessive ISI at 10-Gb/sec.

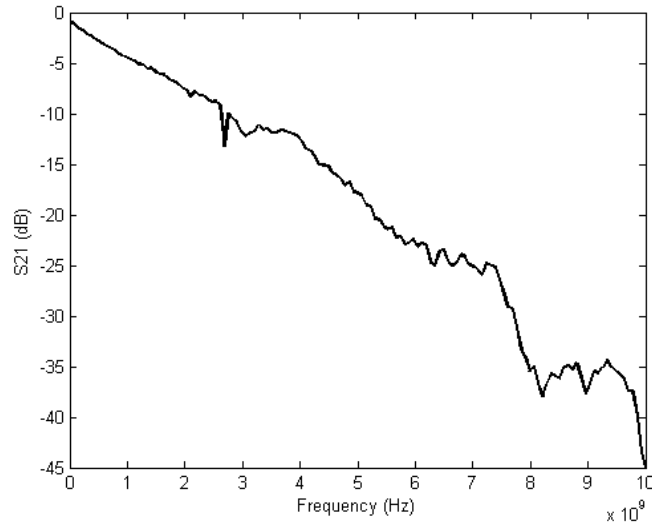
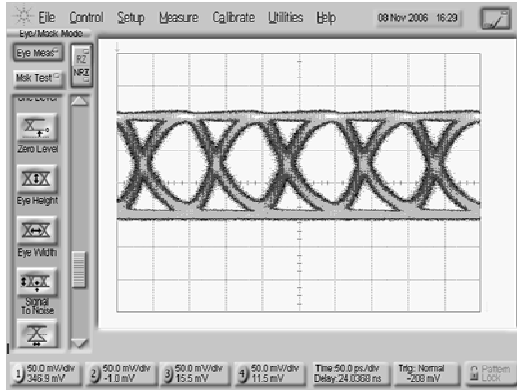
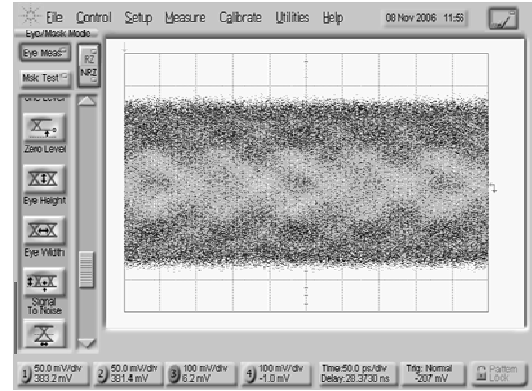


Figure 2.7 S_{21} of 20-inch backplane trace.

As the data rates of the pulse train and the length of the channel increases, ISI becomes so severe that the transmitted data cannot be recovered. The eye-diagram is a composite view of all the bit periods of a captured waveform superimposed on each other and is a useful tool to evaluate signal integrity. The effects of ISI can be seen by looking at the eye-diagram of the signal at the input and output of a 20-inch Tyco backplane channel shown in Figure 2.8. Figure 2.8(a) shows a 10-Gb/sec PRBS signal with open eyes. Although there is some slope to the rise and fall of the transitions, the eye is open at the centre and a decision-making device can correctly receive this data stream. After transmission through the FR-4 channel, severe ISI results in a closing of the eyes, as shown in 2.8(b). The decision-making device cannot distinguish between 1's and 0's resulting in worse BER.



(a)



(b)

Figure 2.8 (a) 10-Gb/sec PRBS input and **(b)** After 20-inch backplane channel.

ISI deteriorates with increasing data rates and channel length. Figure 2.9 shows the eye-diagrams for 2.5-Gbsec, 5-Gb/sec and 10-Gb/sec PRBS signal through a 20-inch backplane trace. At 10-Gb/sec the eye is completely closed. Therefore, legacy backplanes of length 20 inches or more, that were suitable for 1-Gb/sec data transmission, are a bottleneck at 10-Gb/sec. Figure 2.10 shows the eye-diagram for a 5-Gb/sec PRBS $2^{31}-1$ signal through 6 inches and 24 inches of FR-4. The thickness of the eye-lid and the jitter increases for the 20-inch trace, illustrating the effect of channel length on ISI.

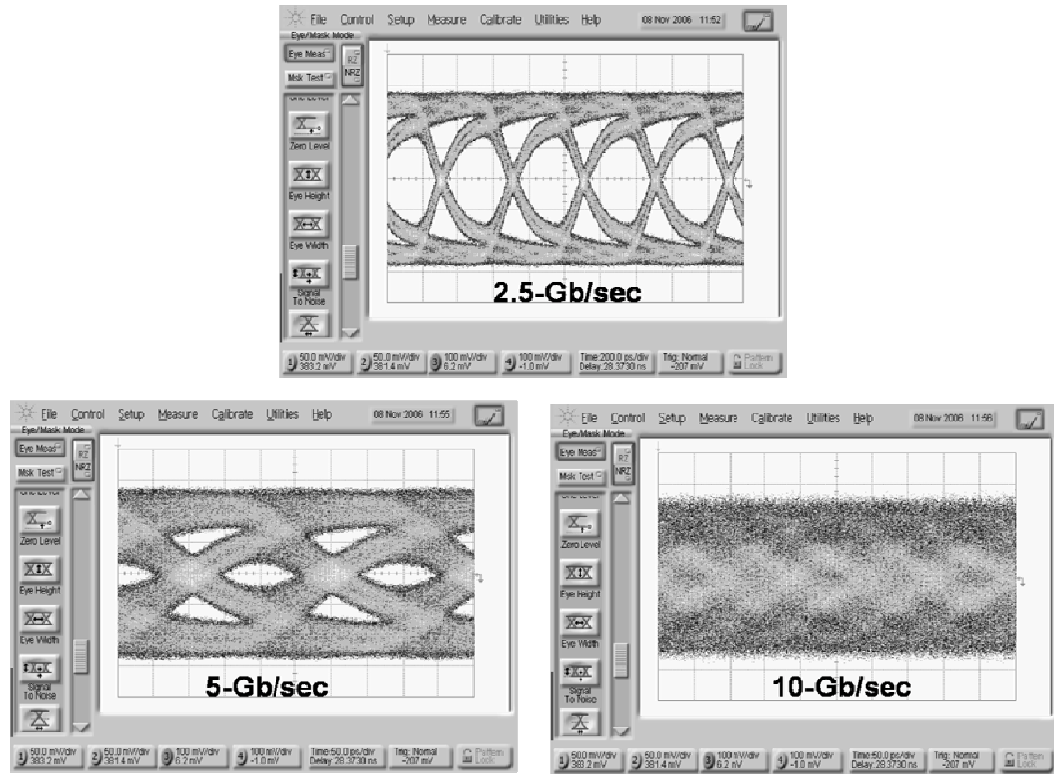
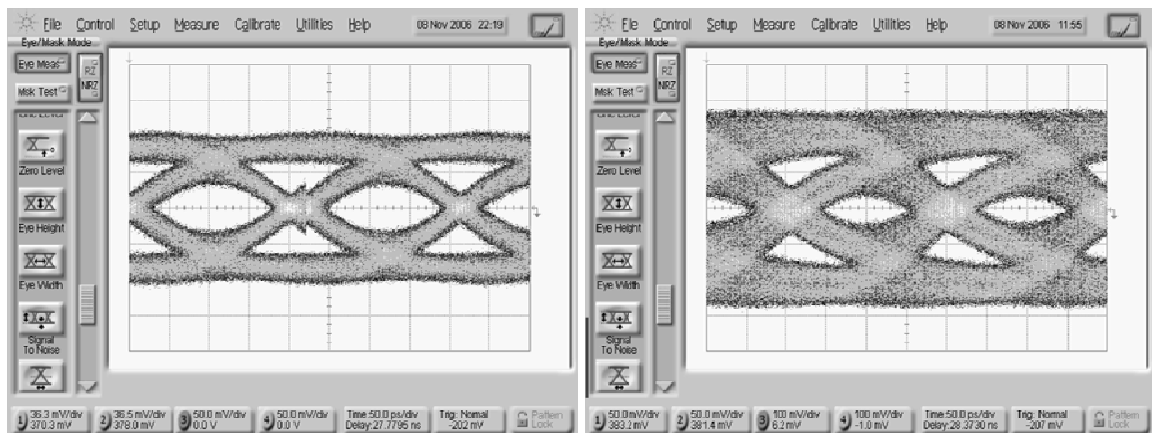


Figure 2.9 Effect of increasing data rate on ISI.



(a)

(b)

Figure 2.10 Effect of channel length on ISI – 5-Gb/sec PRBS through (a) 6-inch and (b) 20-inch backplane trace.

2.3 ISI in Optical Data Transmission Systems

Using the definition of a baseband channel given in the previous section, optical fibre is not a baseband channel since it uses a carrier frequency, namely light. The frequency of the carrier frequency is much higher than RF or microwave carrier frequencies. Typically light of wavelength 850 nm–1550 nm is used in optical fibres. This translates to a frequency in the range of 10^{14} Hz. However, the optical fibre channel, including transmitter, fibre and receiver is considered a baseband channel when it is used to transmit baseband data [2.1]. The most commonly used optical fibre systems use direct-detection, where the power of the light is modulated by a data signal and the detector converts the received power into an electrical current [2.1]. Transmission of baseband data using light is typically done using NRZ on-off keying (OOK) modulation. The digital baseband data is used to modulate the optical output power of a light source, typically a laser or a light-emitting-diode (LED), or an external modulator, such as the Mach-Zehnder (MZ). A “1” translates to an “on” optical pulse and a “0” translates to an “off” optical pulse. The modulated light is then received using a photodetector that translates the modulated light power into an electrical current. Direct detection does not depend on the wavelength of the light being used. The wavelength only determines the attenuation of optical power as it travels down silica fibre. Early optical systems operated around the 850 nm because laser sources available at the time operated at this frequency. The development of laser sources and photodetectors operating around 1300 nm allowed a shift in the transmission wavelength from 800 nm to 1300 nm [2.10]. Systems operating at 1550 nm provide the lowest

attenuation of around 0.2-0.3 dB/km [2.10]. Figure 2.11 depicts a standard plot illustrating fibre attenuation in dB/km for the optical spectrum [2.11].

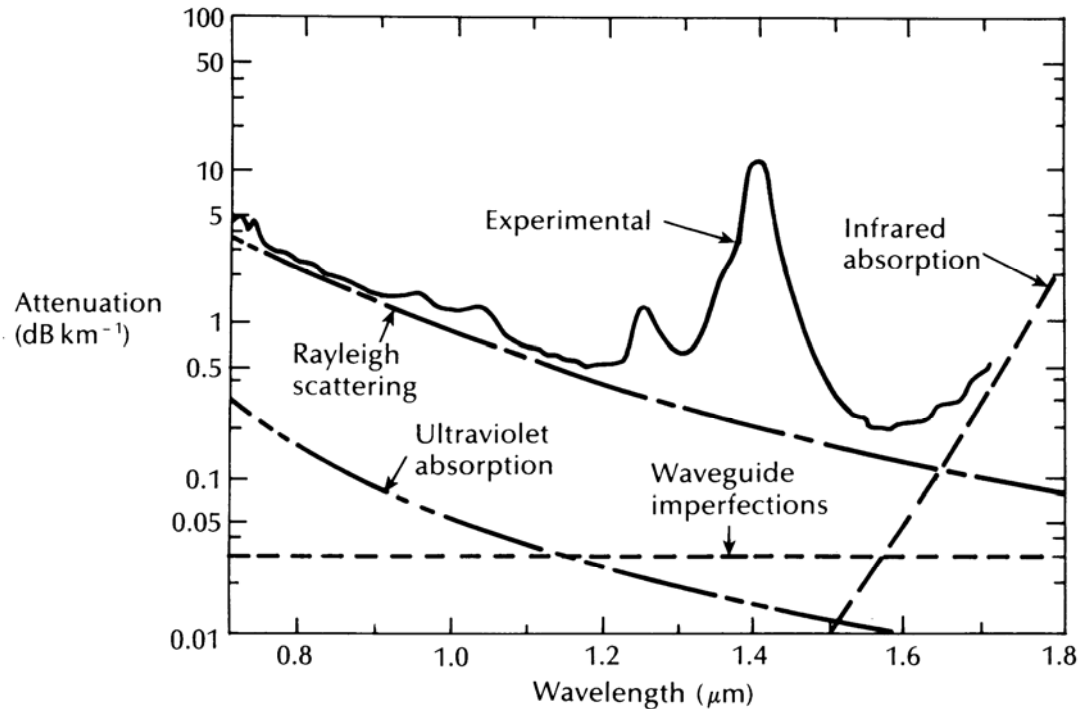


Figure 2.11 Fibre attenuation in dB/km across wavelength [2.11].

Modern fibre optic communications began in 1970, and today optical fibres form the backbone of long-haul MAN, WAN and short-haul LAN networks. The advent of using light as a medium of data transmission dates back to antiquity if we consider the use of fire as a means of signalling in ancient times. More recently, optical communication can be traced to Alexander Graham Bell's photophone in 1880 [1.1]. However, it was not until the 1960's, with the invention of a coherent optical source and optical waveguides to prevent atmospheric interference and ensure the secure transport of light, that his work could be utilized in modern telecommunication and data transmission systems [1.1]. Optical fibre

transmission enabled much higher data rates than copper cables because of the inherent wide bandwidth of light as a carrier. Further advancements, such as the development of high-speed tuneable lasers, electro-optic modulators, photoreceivers, WDM, and the development of high-speed optical transceivers, splitters and repeaters has further increased data rates and enabled wide-spread deployment of fibre-optic networks. Although, theoretically, optical fibres have unlimited bandwidth and should pose no limitations to data rates, optical pulse dispersion in the fibre translates to ISI after opto-electric conversion in the photoreceiver and has become an issue as data rates move to 10-Gb/sec. Dispersion mechanisms vary depending on the type of fibre. The following sub-sections look at the dispersion mechanisms in multi-mode and single-mode optical fibre.

2.3.1 ISI in Multi-mode fibre (MMF)

In multi-mode fibre (MMF), the light travels down the fibre in different modes. The modes travel at different speeds down the fibre core and arrive at the receiver at slightly different times. Lower order modes travel straight down the core of the fibre and have the lowest transit time. Higher order modes travel closer to the cladding of the fibre and have a larger transit time. This is known as differential modal delay (DMD) and results in optical pulse dispersion. After opto-electric conversion in the photoreceiver, this results in ISI in the electrical signal. MMF enables the use of lower cost vertical cavity surface emitting lasers (VCSELs), light emitting diodes (LEDs) and optical connectors compared with single-mode fibre that uses more expensive laser diodes (LDs) and has more stringent coupling requirements. Therefore, historically, MMF has been deployed in lower-cost LAN applications where

the cost of deploying SMF systems is prohibitive. SMF does not exhibit DMD and has a higher data rate capacity. It has therefore found use in long-haul systems that are more expensive to install. MMF has found extensive use in enterprise LANs where links spans are typically less than 500 m. Until recently, the capacity of MMF was ahead of the capability of the related electronics. However, at 10-Gb/sec DMD significantly reduces the reach of installed MMF, introducing challenges as enterprise networks attempt to upgrade to 10-Gb/sec Ethernet. A majority of the fibre that was deployed in LANs is FDDI-grade or OM1 type fibre with a core diameter of 62.5- μm . The data carrying capacity of fibre is defined by its modal bandwidth (-3dB optical bandwidth under certain conditions). FDDI-grade fibre has a modal bandwidth of 160/500 MHz.km at 850/1310 nm. OM1 type fibre has a modal bandwidth of 200/500 MHz.km at 850/1310 nm [1.4]. DMD gets worse at 10-Gb/sec and significantly limits the reach of installed OM1 and FDDI-grade fibre. FDDI-grade fibre only supports 26 m at 10-Gb/sec and OM1 fibre supports 33 m at 10-Gb/sec. To get an idea of what effect this has; more than 60% of fibre links within deployed enterprise backbones span a distance of between 101-300 m and more than 30% of all installed fibre world-wide is either OM1 or FDDI-grade [1.4]. Of course, improved fibre could give the necessary performance. OM2 and OM3 fibre have a core size of 50- μm . A smaller core-size means fewer modes can propagate and therefore results in reduced DMD and ISI. OM2 has a modal bandwidth of 500/500 MHz.km at 850/1310 nm. OM3 type fibre has a modal bandwidth of 2000/500 MHz.km at 850/1310 nm. However, installing entire spans of new fibre is an expensive proposition for enterprise LAN operators and there is a demand for a cost-effective solution to use the existing fibre at the higher data rates. Even

though newer fibre is being slowly installed, at the end of 2007, 30% of installed fibre world-wide will still consist of legacy FDDI-grade or OM1 fibre [1.4]. Therefore, there is a demand for cost-effective solutions to that will enable extending the life-span of the legacy MMF. IC solutions such as electronic dispersion compensators (EDCs) offer more flexibility, lower area and cost than optical techniques like offset launching. With this demand in mind, the 10GBASE-LRM standard was approved requiring EDC technology to enable 10-Gb/sec over legacy FDDI-grade fibre up to 220 m in length.

2.3.2 ISI in Single Mode Fibre (SMF)

Although SMF has much higher data carrying capacity than MMF and has therefore been used extensively in long-haul links, certain dispersion mechanisms causing ISI can limit the reach of fibre spans at 10-Gb/sec data rates and beyond. In a single-mode fibre (SMF), polarization mode dispersion (PMD) and chromatic dispersion (CD) are the main dispersion causing mechanisms resulting in ISI after the photoreceiver. PMD occurs when two polarization modes travel down a fibre at different speeds due to imperfections in the fibre geometry. When they are combined at the photoreceiver, ISI occurs in the electrical domain. CD occurs due to variations in the speed of light of varying wavelengths. After the photoreceiver, dispersion in the optical domain becomes ISI in the electrical domain. CD increases linearly with length and is a static phenomenon. PMD is dynamic and changes with time. PMD and CD can significantly limit the reach of existing SMF at 10-Gb/sec. Dispersion compensating fibres (DCFs) are often used to combat CD. However, such fibres are costly and bulky. PMD is problematic to compensate in the optical domain as it is sensitive to mechanical

vibrations, bending etc. Therefore, compensation techniques have to be adaptive. For these reasons, electronic dispersion compensation (EDC) techniques have been proposed as a cost-effective and compact solution to combat optical pulse dispersion and the resulting ISI in SMF [2.12].

2.4 Equalization

The previous two sections looked at ISI caused by bandwidth limitations in backplanes and dispersion in optical fibres. Even though the causes of ISI differ depending on the channel, the same equalization techniques can be employed for both channels. The next few sub-sections look at ISI and equalization in more detail.

2.4.1 Pre-and Post-Cursor ISI

ISI can be thought of as the effect of past and future symbols on the current symbol. If the signal after a band-limited channel is expressed in discrete time, at time n , the symbol $y[n]$ with ISI can be defined as in (2.14).

$$c_{-m}y[n+m] + \dots c_{-2}y[n+2] + c_{-1}y[n+1] + c_0y[n] + c_1y[n-1] + c_2y[n-2] + \dots c_ly[n-l] \quad (2.14)$$

The equation shows the current symbol $y[n]$ (with some factor c_0) along with some factor ($c_m \dots c_l$) of l past symbols and m future symbols respectively. The roll-off of the rising edge of a pulse can be seen to have an effect on the next bit (bit on the left in a pulse train) and is called pre-cursor ISI. The roll-off of the falling edge of the pulse can be seen to have an effect on the previous bit (bit to right in pulse train) and is called post-cursor ISI. Figure 2.12 illustrates a discrete-time representation of an impulse response with pre- and post-cursor ISI. In a practical system, it is reasonable to assume

that the ISI affects a finite number of symbols. Hence we can assume $c_n = 0$ for $n < -m$ and $n > l$, where m and l are finite, positive integers. The total span of ISI is $L = m+l$.

The impulse response of a channel can also show pre- and post cursor ISI. The impulse response, $h(t)$, of a channel is obtained by taking the inverse Fourier transform of its frequency domain transfer function, $H(f)$. Figure 2.13 shows the impulse response of a dispersive MMF channel showing pre- and post-cursor ISI.

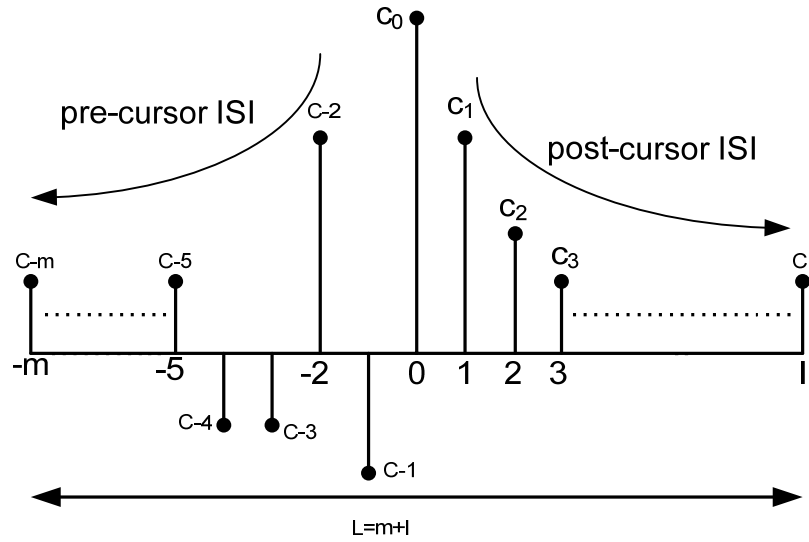


Figure 2.12 Discrete-time representation of pre- and post-cursor ISI.

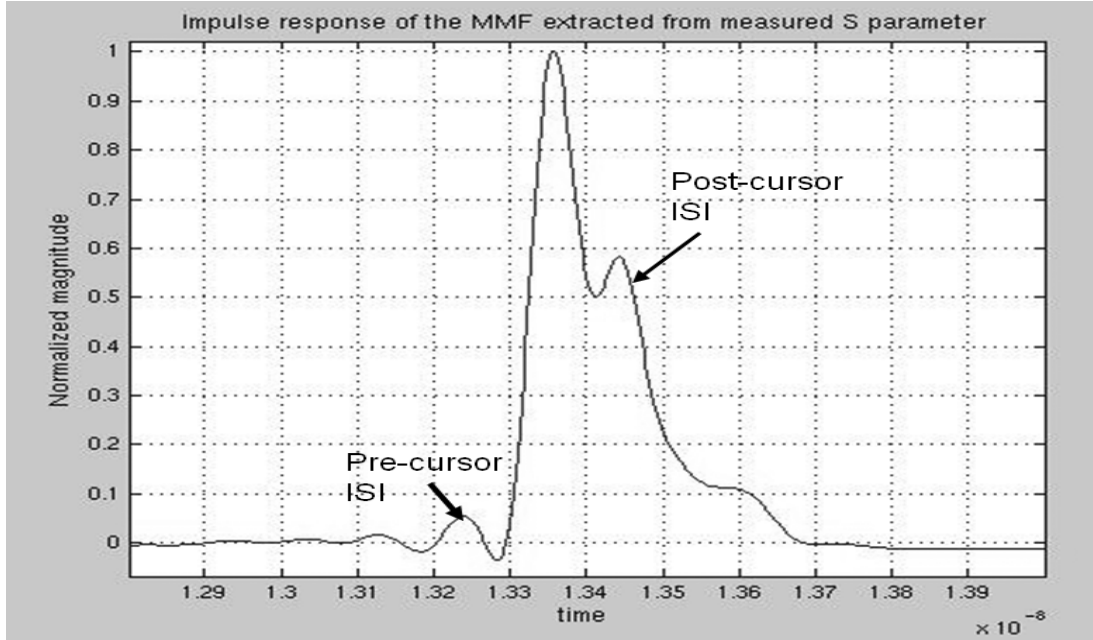


Figure 2.13 Impulse response of a MMF.

2.4.2 Maximum-Likelihood Sequence Detector

The theoretical optimum detector for recovering a data sequence with ISI is the maximum-likelihood (ML) sequence detector [2.1]. The Viterbi algorithm is used to obtain the most likely sequence of symbols. The computational complexity of the Viterbi algorithm is exponential in L . Therefore, this type of detection is only practical when there is limited ISI. For channels with large L , i.e., more ISI, the complexity of implementing the ML sequence detector makes the task impractical. In such cases, sub-optimal methods are used to detect the transmitted symbols in the presence of ISI [2.1]. The next section looks at two commonly used sub-optimal methods: linear and non-linear equalization.

2.4.3 Sub-Optimum Equalization Techniques

Equalization is a signal processing technique to compensate for the channel-induced ISI and recover the original transmitted signal. Linear and non-linear equalization techniques have been explored in the literature to compensate for ISI in various dispersive channels. The following sections look at the different equalization techniques.

2.4.3-1 Feed-Forward Equalization

The simplest equalization technique that has been used over the years is linear feed-forward equalization. Feed-forward equalization typically involves the use of a linear transversal finite impulse response (FIR) filter as shown in Figure 2.14. The FIR filter consists of adjustable tap coefficients, c_0 , c_1 , c_2 , c_3 , with a time delay, τ between adjacent taps. τ can be as large as T , the symbol duration, in which case the FFE is a symbol-spaced equalizer. If $\tau < T$, the FFE is called a fractionally-spaced equalizer. In practice, a fractionally-spaced FFE is used to avoid aliasing when $1/T < 2W$, where W is the channel bandwidth [2.1]. The output of the FFE is a summation of the input signal with delayed versions of itself. Depending on the relative values of c_0 , c_1 , c_2 , and c_3 , the FFE can be used to cancel pre- and post-cursor ISI, only pre-cursor ISI, or only post cursor ISI. The tap coefficients c_0 , c_1 , c_2 , and c_3 are calculated using algorithms designed to meet certain system criteria. The tap control unit (TCU) can constantly monitor the channel output and update the tap-coefficients dynamically.

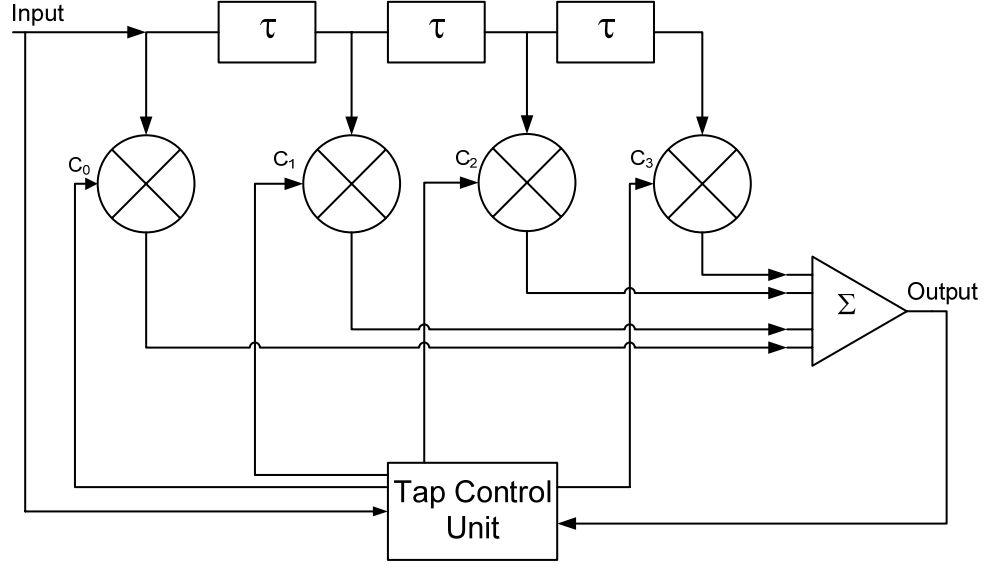


Figure 2.14 Feed-forward equalizer (FFE) topology

The behaviour of the FFE can also be understood in the frequency-domain. In essence, the FFE inverts the channel response so that the total response of the channel and the FFE is flat. So if the channel response $C(f)$, as defined in (2.15), the FFE response $G_E(f)$ is defined as in (2.16).

$$G_E(f) = \frac{1}{|C(f)|} e^{-j\theta_{C(f)}} \quad (2.15)$$

$$|G_E(f)| = \frac{1}{|C(f)|}, \theta_E(f) = -\theta_C(f) \quad (2.16)$$

Equation (2.15) is an illustration of zero-forcing (ZF) equalization. ZF equalization tries to cancel all the ISI in a symbol stream (assuming finite ISI) and results in a transfer function that is the exact inverse of the channel response. The ZF algorithm will extract tap coefficients using the zero-forcing condition [2.1]. While this might sound like an ideal solution, ZF equalization implies gain in the frequency range where the channel response is small. Any additive noise in that frequency range is also amplified. So in noisy channels with deep spectral nulls, the ZF-FFE can result in very poor SNR at the

output. An alternative is the minimum-mean-square-error (MMSE) criterion that aims to relax the zero-ISI criterion and instead tries to minimize the combined power of ISI components and noise components [2.1].

When the FFE is implemented at the transmitter, the process is called pre-emphasis. A pre-emphasis FFE knowingly distorts the transmitted signal so that the combination with the channel distortion results in an ISI-free signal at the output. Pre-emphasis is relatively easier to implement and it can simplify receiver design by providing a relatively open eye at the receiver. However, it has its drawbacks. Pre-emphasis is useful if the channel characteristic is known a-priori and is static, i.e., it does not change with time. However, for a channel that changes with time, the pre-emphasis circuit would need updated information from the receiver, requiring a designated back-channel, or at the least, a parallel channel during the equalizer training period. Furthermore, as IC supply voltages get lower, the output signal of the transmitter is constrained. So most pre-emphasis circuits suppress the lower frequency signal components instead of boosting the high-frequency signal components. This results in a reduced DC level at the transmitter and a small eye at the receiver [2.13]. For these reasons, linear equalization at the receiver has been explored [2.14]. A receiver equalizer can constantly monitor the channel output and update the equalizer tap coefficients dynamically [2.13].

FFE's have been shown to be effective on channels where the ISI is not severe. As mentioned earlier, the FFE amplifies noise on channels with spectral nulls resulting in poor SNR. On certain channels, the FFE has been shown to be insufficient in cancelling ISI [2.15]. Therefore, non-linear equalizers such as the decision-feedback equalizer (DFE) have been explored.

The DFE is a non-linear equalizer that employs previous decisions to eliminate the ISI caused by previous symbols on the current symbol [2.1].

2.4.3-2 Decision-Feedback Equalization

Decision-feedback equalization was first introduced by M. E. Austin in 1967, who introduced a decision-theory approach to solve the problem of digital communication over known dispersive channels [2.16]. This work was the first to describe an approach to use knowledge of past decisions to make corrections to current symbols and thereby cancel post-cursor ISI. With advances in integrated circuit technology, it became possible to implement the decision-feedback equalization functionality in silicon. The DFE was used extensively to combat ISI in disk-drive read channels [2.17]. As data rates in transmission systems increased, DFEs were adopted in multi-Gb/sec data transmission systems to cancel ISI induced by channel loss in copper-based transmission systems [2.13]. DFEs have also been proposed for optical receivers to compensate for DMD, CD, and PMD in multi-mode and single-mode fibres [2.18, 2.19]. The traditional DFE, as shown in fig. 2.15, consists of a forward filter, a clocked decision element, and a feed-back filter. The forward filter is generally implemented as a fractionally-spaced FFE with tap coefficients set to cancel pre-cursor ISI. The feedback filter is a symbol-spaced FIR filter with tap coefficients set to cancel post-cursor ISI. By definition, decision-feedback equalization can only remove post-cursor ISI, i.e., ISI caused by previous symbols. Therefore, a practical DFE usually consists of a feed-forward filter that can remove the pre-cursor ISI and provide some eye-opening to the decision element. The decision element makes a decision at each symbol and sends this symbol information to the feedback filter. The

non-linear feedback filter removes the post-cursor ISI, without enhancing noise, to completely open the eye and reduce jitter. The existence of the feedback filter relaxes the requirements of the feed-forward filter. Without the feedback filter, the feed-forward filter taps are set to cancel pre-and post-cursor ISI. With the feedback filter, the feed-forward filter only cancels the pre-cursor ISI. Therefore, with the addition of the feedback filter, the number of feed-forward taps can be decreased or more pre-cursor ISI can be cancelled with the same number of taps. The tap coefficients of the feed-forward and feed-back filters are selected to optimize a desired performance measure. Least-mean-square (LMS) and MMSE algorithms are often used to obtain DFE tap coefficients. The TCU monitors the channel and adapts the tap coefficients accordingly. Furthermore, the same equalizer circuit can be used for a variety of channels, with the TCU deciding the optimum tap coefficients for each case. The number of taps is determined keeping in mind implementation issues and is usually a trade-off between performance, power and area consumption and implementation feasibility.

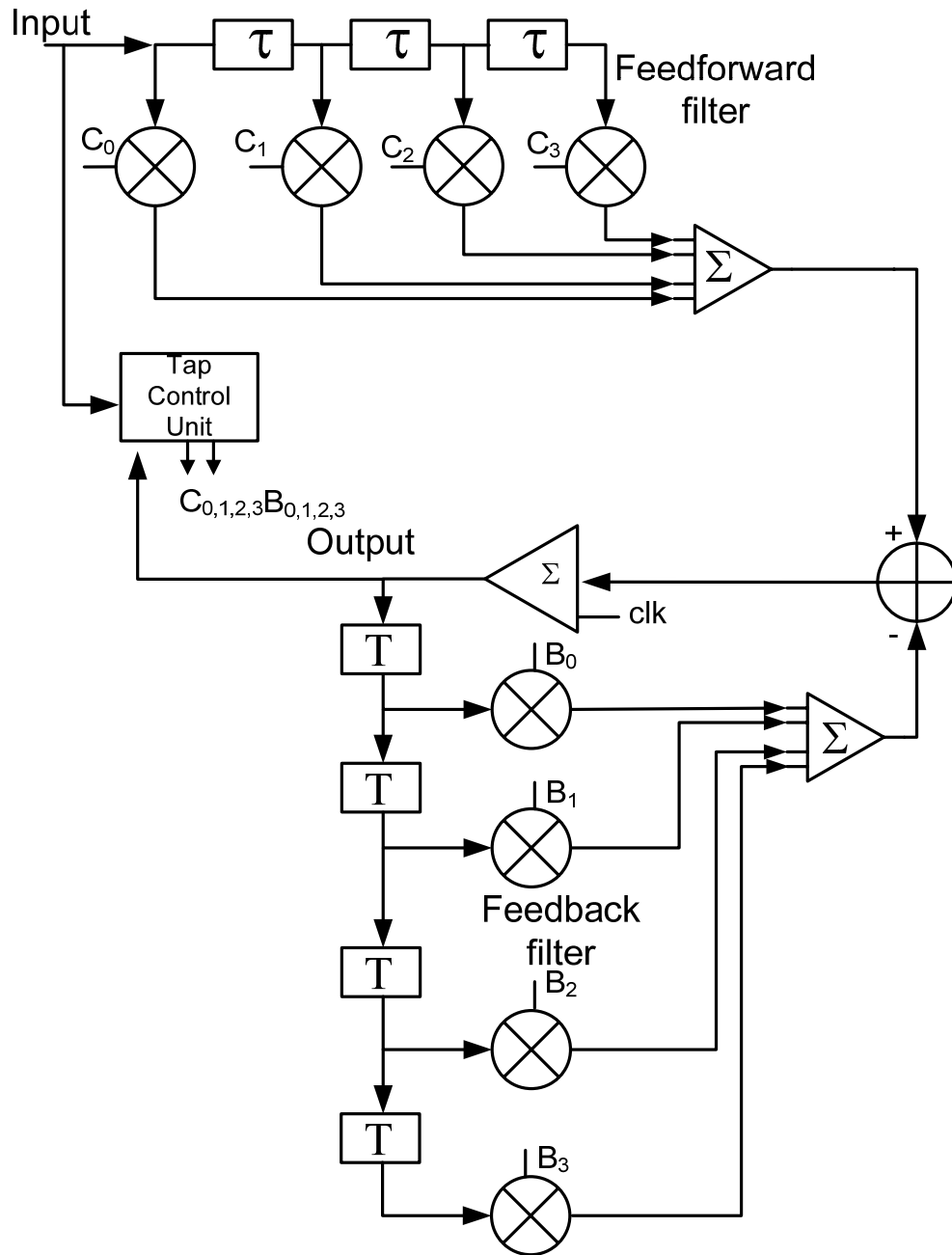


Figure 2.15 Block diagram of decision-feedback equalizer

2.4.4 System Simulations

The improvement in equalization with decision-feedback over and above feed-forward equalization can be demonstrated with system simulations that accurately model the channel and equalizer topology. Several works in literature have shown the value added with decision-feedback. In [2.20] adding one feedback tap (FBT) improves the performance significantly compared to adding more feed-forward taps (FFT) when compensating for PMD in 40-Gb/sec optical links. Similar analysis has been done for FR-4 backplane channels. It has been shown that for certain FR-4 channels at multi-Gigabit data rates, increasing the number of forward filter taps beyond 4 shows no significant improvement and that the DFE significantly improves the voltage margin over a linear equalizer. An equalizer with 3 FFT and 1 FBT achieves a 21% improvement in the eye over an equalizer with 4 FFT and no FBT [2.15].

A MATLAB-based simulator, StatEye, is used to investigate different equalizer topologies and to demonstrate the performance improvement with non-linear decision-feedback equalization. The inputs to the simulator are channel information, usually in the form of frequency-domain magnitude and phase information, data rate, jitter and BER of the input signal, as well as any waveform-shaping filter that may be used, the receiver equalizer topology, including number of taps in the feed-forward and feed-back filter and the algorithm used for tap coefficient extraction. The simulator extracts optimum tap coefficients for the specified channel and equalizer topology. The output of the simulator is the equalizer eye-diagram with information on

jitter and eye-height. Using this information, a figure-of-merit (FOM) for the equalizer is defined as in (2.17).

$$FOM = \frac{\text{eye-height}}{\text{jitter}} \quad (2.17)$$

The equalizer aims to maximize eye-height and minimize jitter. The simulator is used to analyze a MMF fibre channel and the FOM is plotted for various equalizer topologies, as shown in Figure 2.16. The input signal data rate is set to 10.3125-Gb/sec. The channel data is the amplitude and phase response from 0 to 25 GHz of a 300 m long MMF fibre with a 62.5- μm core. The data file is provided by the University of Cambridge and is generated using a set of transformations from modal delay and power data. The source data are generated from a mathematical fibre model and are not empirical fibre measurements. Analytical techniques are used to transform the time domain source data into the frequency domain. The plot shows that the FOM increases initially as the number of forward taps increases. However, after 3 FFTs, the FOM saturates and no further improvement is seen as the number of FFTs increases. The FOM increases significantly as a FBT is added. Further improvement is seen as the number of FBTs is increased. An equalizer with 4 FFTs and 1 FBT improves FOM by 37.9% compared to an equalizer with 6 FFTs, showing that for this channel, adding 1 FBT is better than adding 2 FFTs [2.21]. This simulation illustrates the need for a DFE at 10-Gb/sec for certain channels. The next section describes the challenge of implementing a DFE at 10-Gb/sec in standard CMOS.

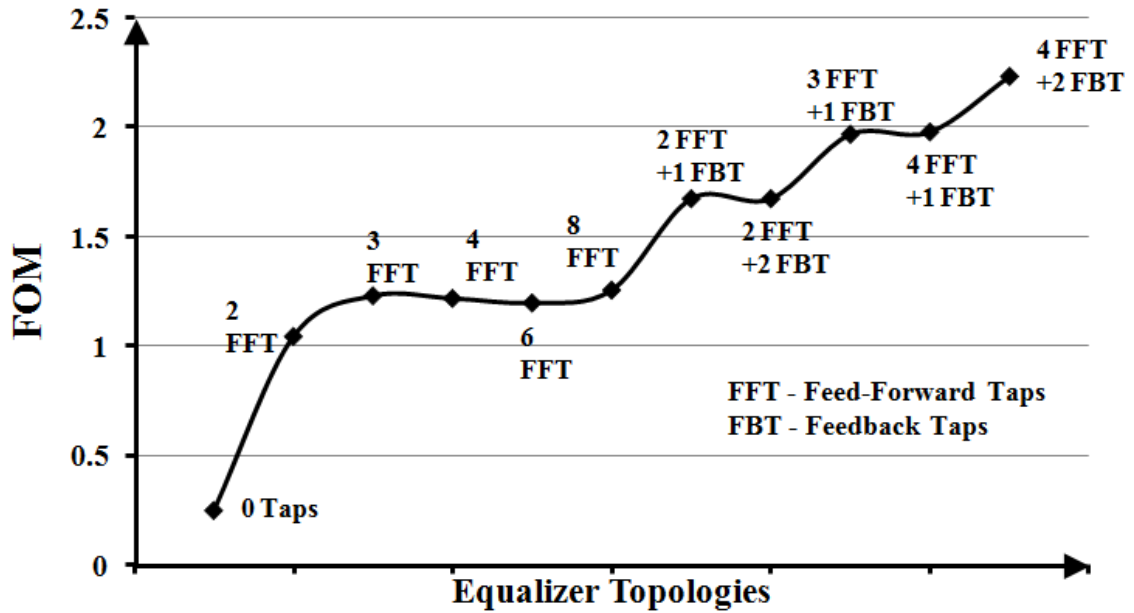


Figure 2.16 FOM for various equalizer topologies [2.21].

2.5 DFE Block Diagram

A concise block diagram of a DFE is shown in Figure 2.17. The DFE is called a non-linear equalizer because of the non-linear decision element, often called a slicer. The slicer is actually a 1-bit ADC and is clocked at the data rate by a system clock. A CDR recovers the system clock from the signal after the forward filter. The output of the slicer is a clean “digital” decision signal. It is “digital” because it has rail-to-rail amplitude and it is timed by the system clock. In modern data transmission systems, non-return-zero (NRZ) signalling is used. So the decision signal is a “1” or a “0”. More specifically, the decision signal is a “high” or a “low”, where the high/low voltage levels vary according to the technology being used. Assuming that this decision is ideally made instantly, the digital decision signal is then delayed by multiples of the symbol duration, T , and used to make a correction to

following symbols. In this manner, the effect of past symbols is removed from the current symbol. The proper operation of the DFE is dependent on the proper functioning of the slicer so that wrong decisions are not fed back to the slicer input resulting in “error propagation”. More importantly, the timing of each loop is critical in order to ensure that ISI caused by the previous symbols is being cancelled at the right time. The number of taps is determined by the amount of post-cursors that need to be removed. It has been shown that cancelling the first post-cursor has the most effect on the output [2.15].

At multi-Gb/sec data rates, digital CMOS circuits used to implement the slicer are a bottleneck in achieving the required speeds. It will be shown that traditional digital CMOS circuits are inadequate or very challenging to implement when data rates increase to 10-Gb/sec and beyond. Up until now, designers have reaped the benefits of CMOS scaling and achieved higher data rates by moving to smaller process nodes. However, the traditional digital circuit architectures become unfeasible at multi-Gb/sec data rates and new techniques and circuit architectures need to be developed to continue the use of standard CMOS. In particular, analog signal processing techniques like current-mode-logic (CML) and unclocked circuit architectures are looked at. The next chapter looks at the challenges of implementing multi-Gb/sec circuits in standard CMOS and explain some of the analog circuit techniques used to overcome the challenges.

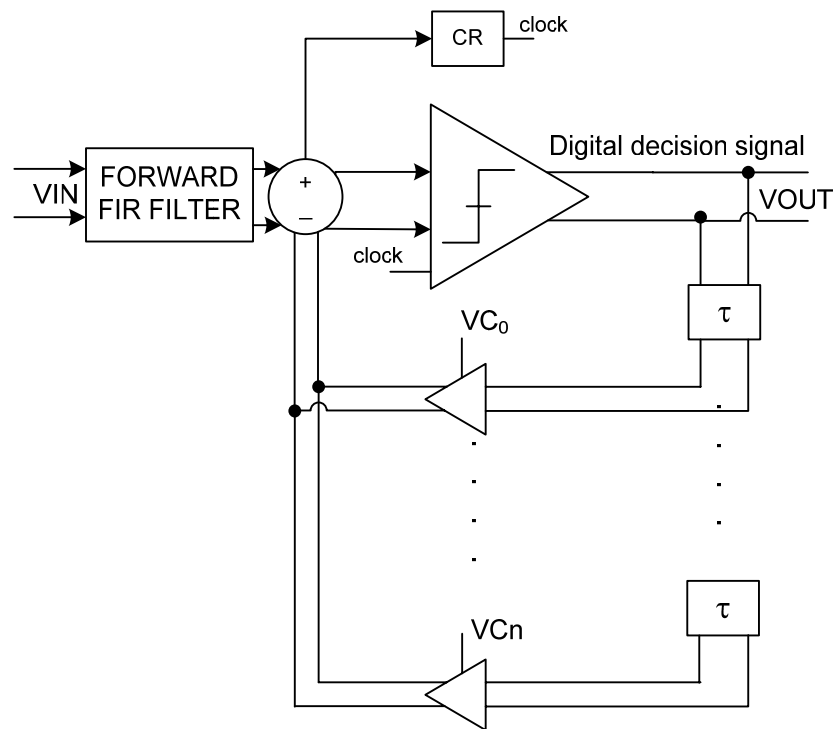


Figure 2.17 Concise block diagram of DFE.

CHAPTER 3

DESIGN CONSIDERATIONS AND TECHNIQUES FOR MULTI-GB/SEC CMOS EQUALIZER DESIGN

3.1 Challenges of Digital CMOS Circuits at Multi-Gb/sec Data Rates

During the past 25 years, silicon CMOS technology has witnessed shrinking device dimensions, increased density, increased speeds and lower costs. The advantages of high-levels of integration and lower cost have made CMOS the technology of choice for ICs in high-speed baseband data transmission systems. Scaling of CMOS processes has enabled designers to re-use existing designs at smaller process nodes to operate at faster speeds with relatively low levels of re-design. As such, several basic circuit architectures have remained constant as data rates progressed from 100's of Mb-sec to 1-Gb/sec. However, as data rates move from 1-Gb/sec to 10 Gb/sec, designers are finding that this fact is no longer true. At multi-Gb/sec data rates, several limitations linked to the process technology make traditional digital circuit architectures challenging to implement using standard CMOS. In addition, as transistor channel lengths decrease to less than 100 nm, increase in static power dissipation places a limit on the integration level and transistor switching speed. This means that traditional digital circuit

architectures that rely on rail-to-rail operation of CMOS logic gates are becoming increasingly difficult and power hungry to implement at smaller process nodes. In fact, most multi-Gb/sec circuits are currently making use of parallelism, with individual circuits being clocked at half or quarter the operating data rate. Fractional-rate clocking enables the use of traditional circuit topologies but results in increased power and area consumption. Therefore, novel analog techniques and circuit architectures are being developed for certain applications. Analog signal processing of baseband data is not limited by limitations imposed by the clock speed and the rail-to-rail operation of digital circuits and can therefore achieve much higher speeds than digital signal processing on the same process node. The ADFE presented in the next chapter is an example of a novel analog circuit architecture developed in response to limitations faced by the traditional digital DFE architecture at multi-Gb/sec data rates. The next section looks at the implementation limitations of the traditional DFE circuit topology.

3.1.1 Multi-Gb/sec DFE

In order to cancel ISI due to the first post-cursor (symbol immediately preceding the current symbol), the slicer (decision circuit) must make this decision and feed it back to its input within T , where T is the symbol duration. The function of the slicer is to sample a continuous-time analog signal, with a peak-to-peak voltage less than 50 mV at every clock period and output a “digital” decision signal. This decision signal is then fed back through the feedback loop. The total timing budget of the first feedback loop is given in (3.1) [3.1].

$$T_{loop} = T_{clk-data} + T_{set-up} + T_{DFE-delay} \quad (3.1)$$

where $T_{\text{clk-data}}$ is the clock-data-delay of the comparator, which includes the time to regenerate a small analog signal to digital CMOS levels, $T_{\text{set-up}}$ is the set-up time of the comparator and $T_{\text{DFE-delay}}$ is the delay through the feedback filter. While this topology worked well when data rates were in the Mb/sec range, limitations in transistor speeds pose a roadblock at multi-Gb/sec data rates. Due to CMOS process limitations, $T_{\text{clk-data}}$ takes up a significant portion of the timing budget at multi-Gb/sec data rates and is a key stumbling block to implementing the traditional digital DFE. The speed of operation of a clocked digital circuit is heavily dependent on the magnitude of the input signal. The output signal levels are 0 and V_{DD} . If the input is also a digital signal, i.e its signal swing is from 0 to V_{DD} , the speed of operation through the circuit is faster than if the input is a small analog signal. The time taken to output a digital CMOS decision when the input is a small analog signal is the critical stumbling block of the decision circuit. Due to this latency challenge in the first feedback loop, implementation of a 10-Gb/sec DFE is a significant challenge to circuit designers. The next section looks at a typical track-and-latch type comparator that is used commonly to implement the slicer in the DFE. It will be shown that the operating speed of the comparator is basically limited by the process technology [3.2].

3.1.2 Track-and-Latch Comparator

Typically, the slicer, which is essentially a 1-bit ADC, is implemented as a clocked track-and-latch comparator. The comparator usually has one or two stage of pre-amplification followed by a track-and-latch stage. Figure 3.1 shows a schematic of a typical CMOS regenerative track-and-latch comparator that is often used to implement the slicer. The pre-amplifier

amplifies the input signal and is used to improve the input dynamic range of the 1-bit ADC. However, the output of the pre-amplifier is still not large enough to drive CMOS digital circuitry. The regenerative track-and-latch stage then amplifies the signal to CMOS digital levels. At every clock cycle, positive feedback is enabled during the latch stage and the comparator “regenerates” the small input differential signal, V_1 - V_2 to a rail-to-rail signal at the output. When clock is low, the PMOS transistors, M_{P1} and M_{P2} , pull the output nodes, $vo1$ and $vo2$, to V_{DD} . This is the track state. When the clock goes high, the NMOS transistors M_{N3} and M_{N4} turn on and positive feedback is enabled with transistors M_{N5} , M_{N6} , M_{P3} , and M_{P4} . Whatever voltage difference is there between V_1 and V_2 is amplified to a full-scale digital signal at $vo1$ and $vo2$. The track/latch comparator is often followed by a SR-latch to store the previous state values during the track state.

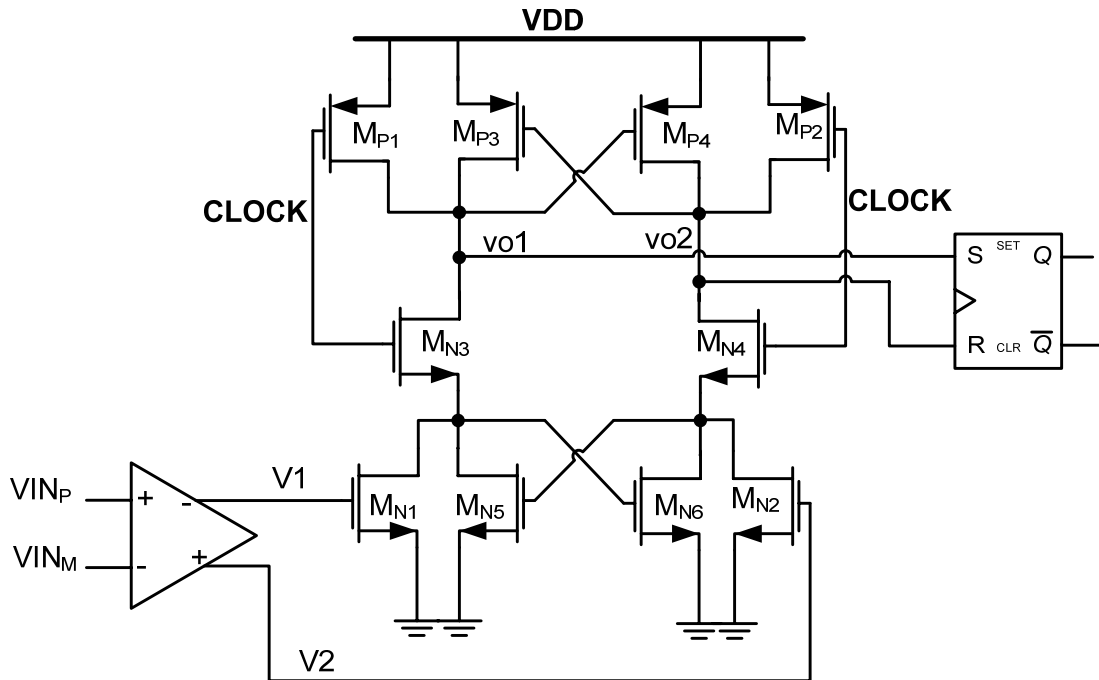


Figure 3.1 Schematic of track-latch comparator.

At multi-Gb/sec data rates, implementing this circuit poses fresh challenges to the circuit designer due to process constraints. The regenerative portion (M_{N5} , M_{N6} , M_{P3} , and M_{P4}) can be modelled as two back-to back inverters as shown in Figure 3.2.

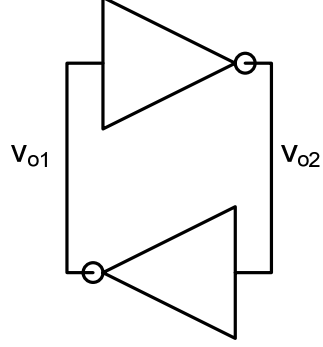


Figure 3.2 Back-to back inverters – model of regenerative transistors.

Assuming that the inverters are in the linear range, and that the output voltages of the inverters are close to each other at the start of the latch phase, the inverters can be modelled as voltage controlled current sources driving an RC load [3.2]. Figure 3.3 shows schematics of this representation.

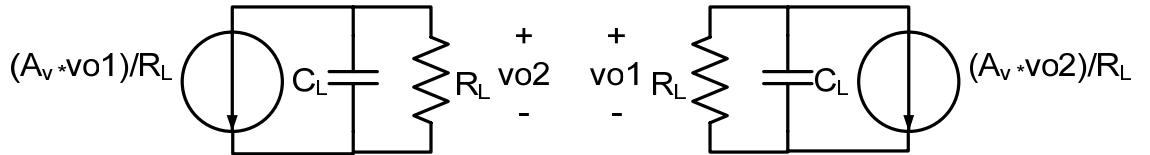


Figure 3.3 Inverters modelled as voltage-controlled current sources.

A_V is the low-frequency gain of each inverter and $G_m = A_V/R_L$. For the linearized model, the following equations hold true [3.2].

$$\frac{A_V}{R_L} v_{o1} = -C_L \left(\frac{dv_{o2}}{dt} \right) - \left(\frac{v_{o2}}{R_L} \right) \quad (3.2)$$

$$\frac{A_v}{R_L} v_{02} = -C_L \left(\frac{dv_{01}}{dt} \right) - \left(\frac{v_{01}}{R_L} \right) \quad (3.3)$$

After some manipulation [3.2], the following holds true.

$$\frac{\tau}{A_v - 1} \left(\frac{d\Delta V}{dt} \right) = \Delta V \quad (3.4)$$

$\tau = R_L C_L$ and is the time constant at the output node of each inverter.

$\Delta V = v_{01} - v_{02}$ and is the voltage difference between the output voltages of the inverters. Its solution is given by (3.5) [3.2].

$$\Delta V = \Delta V_0 e^{(A_v - 1) \frac{t}{\tau}} \quad (3.5)$$

ΔV_0 is the initial voltage difference at the beginning of the latch phase.

Therefore, ΔV increases exponentially with time with a time constant τ_{LATCH} .

$$\tau_{LATCH} = \frac{\tau}{A_v - 1} \cong \frac{R_L C_L}{A_v} = \frac{C_L}{G_m} \cong \frac{1}{f_t} \quad (3.6)$$

The load capacitance is basically the gate source capacitance of the transistors and can be modelled as (3.7).

$$C_L = K_1 C_{OX} W L \quad (3.7)$$

The inverter transconductance is proportional to the transistor transconductance and is given by (3.8).

$$G_m = K_2 g_m = K_2 \mu_n C_{OX} \frac{W}{L} V_{eff} \quad (3.8)$$

Using (3.7) and (3.8) in (3.6) gives, (3.9).

$$\tau_{latch} \cong \frac{K_3 L^2}{\mu_n V_{eff}} \quad (3.9)$$

$$T_{latch} = \tau_{latch} \ln \left(\frac{\Delta V_{final}}{\Delta V_0} \right) \quad (3.10)$$

τ_{latch} is the latch time constant and is basically a function of process parameters [3.2]. The designer has some control over V_{eff} and transistor length, L . The time to regenerate the input voltage to the final output voltage of ΔV_{final} is given by T_{latch} and is a function of the latch time constant, the

initial voltage difference and the final voltage swing required. (3.10) implies that the transition time of a 1-bit ADC is primarily limited by process parameters. For a 0.18- μm CMOS process, τ_{latch} is about 20 ps. Assuming ΔV_{final} is 1.8 V and ΔV_0 is 25 mV, T_{latch} is 85 ps. Therefore, the maximum clock speed of this circuit in a 0.18- μm CMOS process is about 6 GHz. Although different designs may use different type of slicer circuits, this derivation is a good example to show that 1-bit ADCs face speed limitations at 10-Gb/sec data rates due to the process f_t . The literature reviewed shows that even DFEs implemented in 90 nm CMOS do not meet the timing requirements for 10-Gb/sec data transmission without using some technique to overcome the latency requirement. The next section will review some state-of-the-art DFE implementations that have been developed to overcome the critical first feedback-loop latency bottleneck.

3.1-3 State-of-the-Art DFE Implementations

In order to overcome the first feedback loop latency challenge imposed by the limitations of the clocked topology and silicon process f_t , designers have come up with some clever design techniques to implement multi-Gb/sec DFEs in standard CMOS. A commonly used technique in several DFEs is called “look-ahead”, “speculation”, “pre-calculation”, or “unrolling” [3.1], [3.3]. The “look-ahead” concept was first introduced by Kasturia in 1991 [3.4]. The block diagram explaining the concept is shown in Figure 3.4. The basic concept behind this technique is that for a NRZ signal, every symbol is a 1 or a -1/0. The comparator threshold for both possibilities is known. Therefore, the correction to be made to the next symbol is added to the input signal X_N , for both possibilities and sliced to a decision value. So at every clock cycle,

two comparators make two separate decisions using two separate threshold values, α_n and $-\alpha_n$, assuming the previous bit to be a 1 or a -1. The correct decision is then selected using a multiplexor that is controlled by the previous decision a_{n-1} . Since the selecting of a multiplexor input involves all digital CMOS signals, this is a relatively fast operation compared to dynamic decision making from a small analog signal. Assuming standard Boolean values and operators, and looking at Figure 3.4, the n^{th} decision a_n can be expressed as in (3.11) [3.4].

$$a_n = A_n a_{n-1} + B_n \overline{a_{n-1}} \quad (3.11)$$

Similarly, the $n-1^{\text{th}}$ decision can be written as in (3.12) [3.4].

$$a_{n-1} = A_{n-1} a_{n-2} + B_{n-1} \overline{a_{n-2}} \quad (3.12)$$

Substituting (3.12) in (3.11), a_n can be expressed as in (3.13).

$$a_n = A_n (A_{n-1} a_{n-2} + B_{n-1} \overline{a_{n-2}}) + B_n \overline{(A_{n-1} a_{n-2} + B_{n-1} \overline{a_{n-2}})} \quad (3.13)$$

$$a_n = f_1(n) a_{n-2} + f_2(n) \overline{a_{n-2}} \quad (3.14)$$

$$f_1(n) = A_n A_{n-1} + B_n \overline{A_{n-1}} \quad (3.15)$$

$$f_2(n) = A_n B_{n-1} + B_n \overline{B_{n-1}} \quad (3.16)$$

(3.14) shows that a_n is now a function of a_{n-2} and not a_{n-1} . This implies that the critical timing path has been extended from T to $2T$ [3.4]. The multiplexing operation is a relatively fast operation since it involves the delay through one AND gate and one OR gate and operates on large digital signals. However, this approach requires two comparators to detect one symbol as well as the extra multiplexor and therefore results in added area and power consumption. This scheme has been used in virtually all multi-Gb/sec DFE implementations over the past few years. However, at speeds great than 5-Gb/sec even this approach is not sufficient to meet the timing requirements of the first feedback loop.

In addition to the look-ahead architecture, half-rate or quarter-rate clocking is also used to relax the settling time criteria of each comparator. Parallelization however, results in increased area and power consumption. [1.5] demonstrated a 10-Gb/sec DFE in 90-nm CMOS using half-rate clocking and speculative feedback for the first feed-back tap. This means that each slicer is operating at 5-Gb/sec and the critical timing path for the first loop is 400 ps. [3.5] uses quarter-rate clocking and speculation on the first tap to achieve 10-Gb/s operation in 90-nm CMOS. The analysis and information from literature illustrate that the clocked topology and the process f_t is a limiting factor in implementing traditional clocked DFEs at 10-Gb/sec. The next section looks at current-mode logic (CML) circuit techniques and topology to alleviate this timing bottleneck. CML is a high-speed analog circuit technique that overcomes the speed limitations of CMOS logic gates.

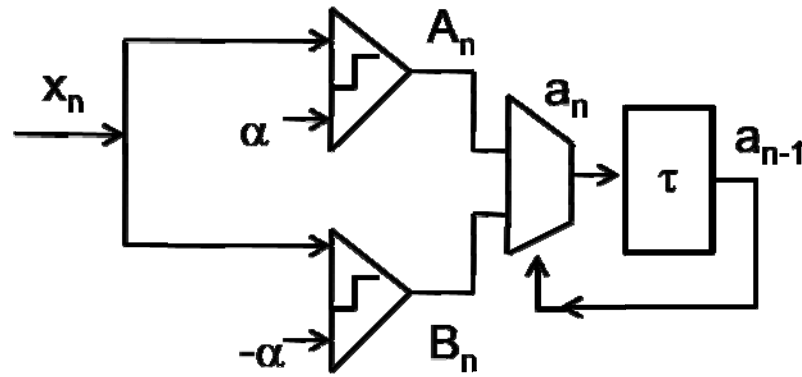


Figure 3.4 Loop unrolled DFE.

3.2 CMOS Current-Mode-Logic (CML) Circuit Techniques

With increasing data rates, CMOS CML circuits are replacing traditional CMOS digital logic circuits for processing high-speed baseband signals. CMOS CML circuits take advantage of the differential signalling scheme used in most baseband data transmission applications. In contrast, CMOS digital logic gates, inverters, and flip-flops are single-ended circuits and are characterized by rail-to-rail operation, large noise margins, very low static power dissipation and compact layouts [3.6]. The rail-to-rail operation is typically achieved by complementary NMOS and PMOS as shown in Figure 3.5. During a transition, only one transistor is turned on, but the load capacitance of both gates is always present. When the input signal is low, the PMOS turns on and the output node is “pulled up” to the V_{DD} rail. When the input signal is high, the NMOS turns on and the output node is “pulled down” to the ground rail. Since they are single-ended, digital CMOS gates are sensitive to supply noise and ground bounce. To implement differential circuits, designers typically use two identical digital cells in parallel. CMOS gates have been used extensively so far in broadband circuits because of their convenient availability in standard cell libraries, low static power consumption, and compact layout area [3.7]. However, at multi-Gb/sec data rates, the input capacitances of the transistors make the switching speed of the pull-up and pull-down operation a bottleneck. Furthermore, supply noise and ground bounce are a significant bottleneck at multi-Gb/sec data rates. For these reasons CMOS CML circuits have been investigated for use in multi-Gb/sec baseband circuits.

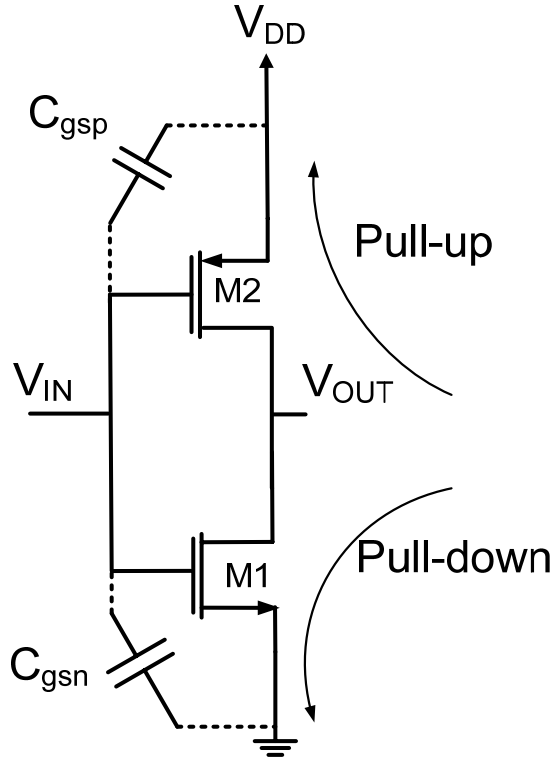


Figure 3.5 CMOS inverter.

A CMOS CML circuit has the topology shown in Figure 3.6. It is basically a CMOS differential amplifier and it is assumed that during CML operation, the input signal, V_{IN} , is large enough to completely switch the tail current, I_{SS} , to one side or the other. In essence, it is a non-linear analog circuit. It is non-linear because although the differential pair is biased around a common-mode voltage, the input signal is not considered small-signal during CML operation. In small-signal operation, the output voltage is determined by small signal gain, A_v . As long as the input signal is within the small-signal input dynamic-range of the differential pair amplifier, and assuming ideal square-law behaviour, A_v is given by (3.17). V_{OUT} is given by (3.18).

$$A_V = g_m R = R \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} \quad (3.17)$$

$$V_{OUT} = A_V V_{IN} \quad (3.18)$$

For CML operation, the minimum differential voltage V_{min} , required to fully switch the entire tail current to one side is given by: [3.6]

$$I_{SS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{min}^2 \rightarrow V_{min} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \quad (3.19)$$

When the circuit is operating in large-signal mode, the output voltage is given by (3.20)

$$V_{OUT} = V_{DD} - I_{SS} R \quad (3.20)$$

The time constant of the CML circuit is given by (3.21).

$$\tau = kRC_l = RkWL C_{ox} \quad (3.21)$$

k is related to physical constants and transistor dimensions. C_l depends on NMOS gate and drain capacitances. The values of I_{SS} and R can be set depending on the V_{OUT} required. The V_{min} required for CML operation is then determined by (3.19). If the circuit needs more dynamic range, i.e, a smaller V_{min} , I_{SS} can be decreased. Accordingly, R will have to be increased to maintain the V_{OUT} . Since the CML circuit is a differential circuit, it has the advantage of high-common-mode rejection and is therefore less sensitive to supply noise and ground bounce than a static CMOS gate. Furthermore, the load presented by a CML cell is the gate capacitance of a single NMOS transistor, unlike in the static CMOS gate. CMOS CML has the advantage of faster switching speeds and smaller output swing than CMOS logic gates. Rail-to-rail operation is not required for most CMOS baseband circuits, and it is the time taken for the signal to reach the rail voltage that is the bottleneck in multi-Gb/sec circuits. When cascaded stages of CML circuits are used,

high-speed small analog signals can be driven to large signal levels if the stages are designed so that $V_{OUT} \geq V_{min}$ of the next stage. CML circuits are suitable for multi-Gb/sec baseband circuits where a clocked digital circuit would exhibit speed limitations. Therefore, CML circuits have been used in the ADFE.

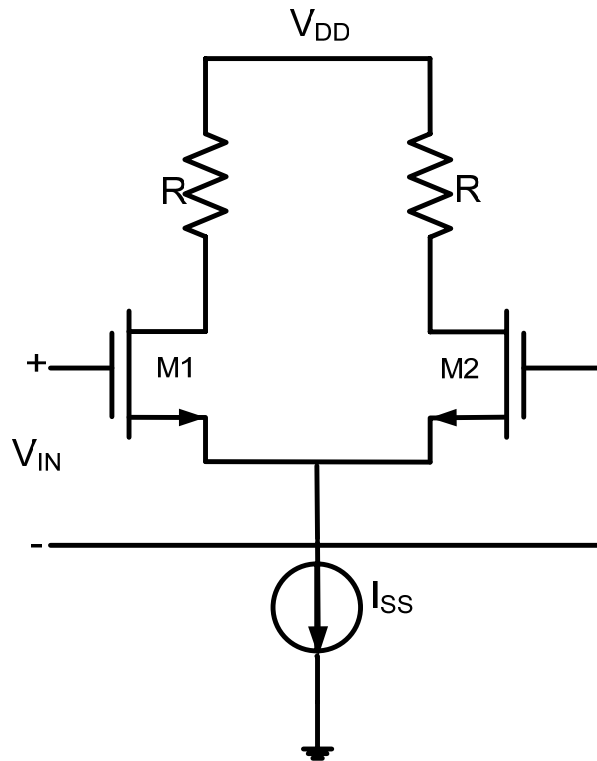


Figure 3.6 CML circuit.

The linear equalizer (LE) is a necessary part of the complete DFE. The taps of the LE, which is implemented as a FFE, are set to remove pre-cursor ISI and when the received eye is severely deteriorated, non-linear decision-feedback equalization is useless without linear feed-forward equalization. The DFE decision block needs some eye-opening in order to make a decision. The next section looks at the design of the linear FFE.

3.3 Feed-Forward Equalizer Design

The primary building blocks of the analog FFE, as shown in Figure 3.7, are a linear variable gain amplifier (VGA) for the tap coefficients, a linear tuneable delay cell for the delay between each tap, and a summing node to combine the outputs of each tap. The VGA and delay cells are linear circuits because they deal with small signals and the transistors operate in the saturation region to give linear gain. Small-signal equations and transistor models are valid for the linear equalizer design. The following sections highlight the design challenges and trade-offs that exist in implementing a 10-Gb/sec analog FFE. The challenges of implementing a multi-tap analog equalizer are illustrated as reasons for implementing the DFE in order to relax the requirements of the linear equalizer. The VGA is implemented using a Gilbert cell topology and the delay cell is implemented using active differential pair cells with a voltage-controlled tuneable delay feature [3.8]. The summing node is implemented using passive resistors to enable high-speed operation.

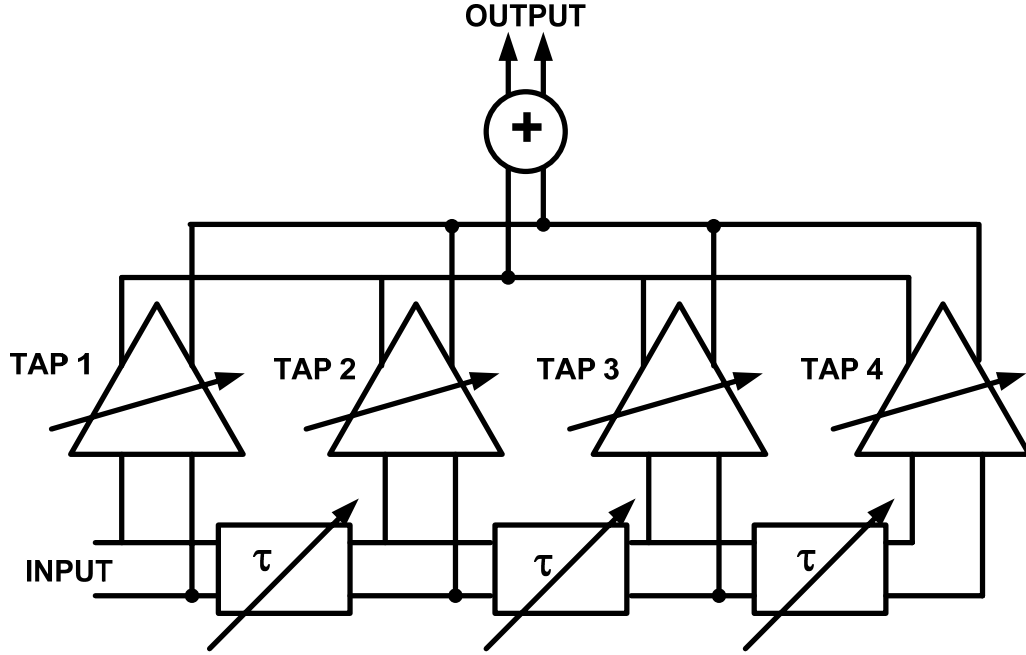


Figure 3.7 Block diagram of FFE.

3.3.1 VGA

The VGA is implemented using a Gilbert cell structure as shown in Figure 3.8. The goal of the VGA is to provide a linear gain of at least +1 to -1. The cross-coupled NMOS input pair with inputs tied together produces this bipolar gain. The small signal gain is determined by $-(g_m + g_{mbs}) * R$, where g_m and g_{mbs} are the small-signal transconductance and bulk-source transconductance of transistors M1-M4. Variable bipolar gain is obtained by controlling the ratio of the two bias currents, I_{BIAS1} and I_{BIAS2} . For zero gain, $I_{BIAS1} = I_{BIAS2}$. For maximum positive gain $I_{BIAS2} = I_{BIAS}$ and $I_{BIAS1} = 0$. For maximum negative gain $I_{BIAS1} = I_{BIAS}$ and $I_{BIAS2} = 0$. In-between ratios of I_{BIAS1} to I_{BIAS2} will produce intermediate values in gain. A voltage-controlled folded gain-control scheme controls I_{BIAS1} and I_{BIAS2} and is used to alleviate the voltage headroom constraint present in the traditional Gilbert Cell topology.

[2.15]. The external control voltage V_{CONT} controls the flow of bias current I_{BIAS} through transistors M5 and M6. Current-mirroring is used to control the ratio of the Gilbert cell bias currents, I_{BIAS1} and I_{BIAS2} in M9 and M10 [2.15].

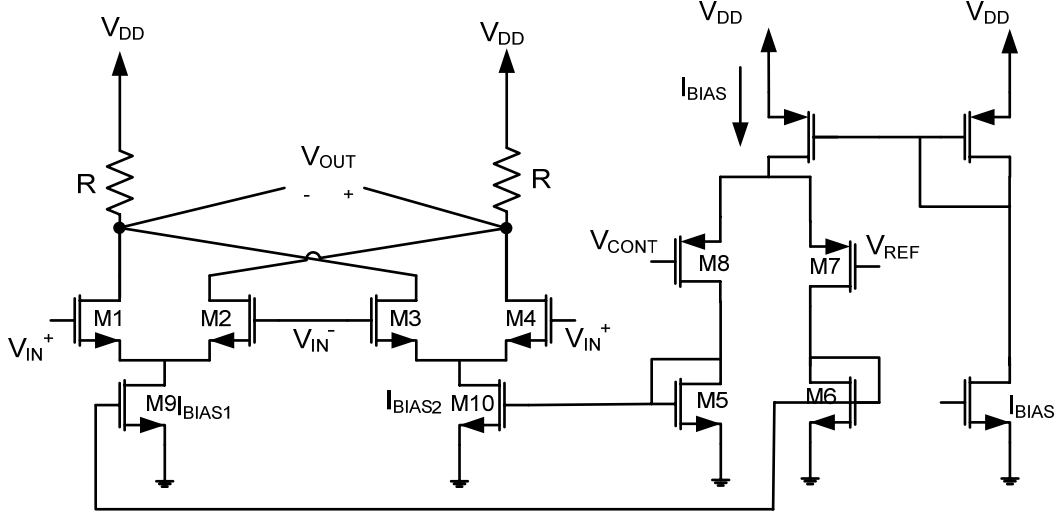


Figure 3.8 Schematic of Gilbert cell with folded gain control.

The drains of all the Gilbert cell transistors are tied together at the summing node and resistive loads are used to perform summing in the current domain as shown in Figure 3.9. The bias current I_{BIAS} , is determined by the number of taps that need to be tied together. Increasing I_{BIAS} can improve bandwidth as the load resistor and transistor sizes can be decreased, while maintaining the same gain. However, the total current flowing through the load resistors is given by (3.22). V_{DROP} is the voltage drop across each load resistor.

$$I_{\text{TOTAL}} = n \times I_{\text{BIAS}} \quad (3.22)$$

$$V_{\text{DROP}} = n \times I_{\text{BIAS}} \times R \quad (3.23)$$

The voltage drop across the load resistors is V_{DROP} at all times, even when the taps are off. The common-mode voltage at the summing node, $V_{\text{OUT,CM}}$, needs

to be high enough so that the input transistors maintain operation in the saturation region. So n and I_{BIAS} are limited by (3.24).

$$V_{DD} - (n \times I_{BIAS} \times R) \geq V_{DSAT} \quad (3.24)$$

This implementation limitation is one of the key motivations for the DFE. Many applications may show improved performance in system simulations by increasing the number of linear equalizer taps. However, if the linear equalizer is to be implemented in the analog domain, the voltage headroom of the multiplier cells limits the number of taps that can be implemented. Increasing the number of taps, n , will require decreasing I_{BIAS} to maintain the same V_{OUT} common-mode voltage. This would mean increasing the transistor width, W or load resistor, R to keep the gain constant. This would mean decreasing bandwidth. The bandwidth-headroom trade-off is the key design challenge for the linear equalizer VGA.

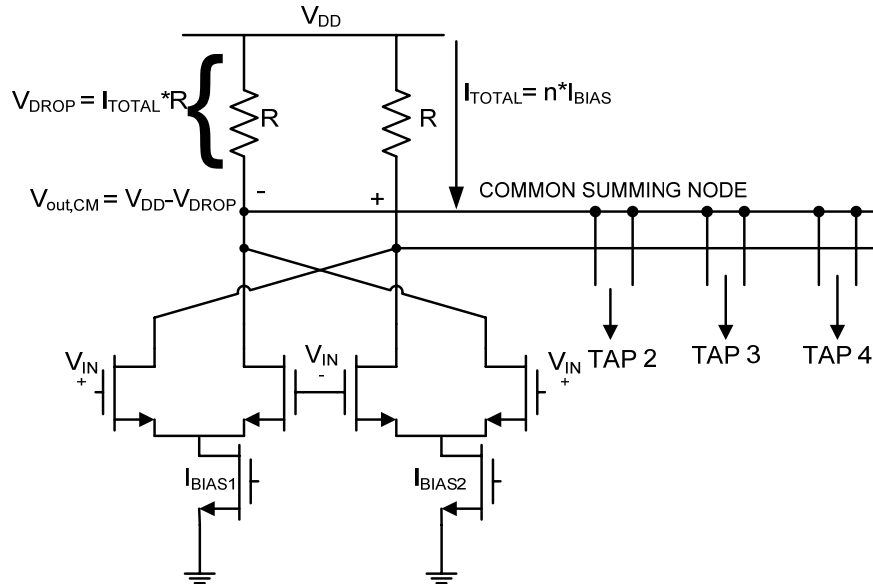


Figure 3.9 Schematic of the Gilbert cell.

The simulated frequency response of the VGA is shown in Figure 3.10. The load resistor used is the summing node resistor and the load capacitance consists of the drain capacitance of another VGA as well as the input capacitance of the DFE. The 3-dB bandwidth under these conditions is 11.5 GHz. Obviously, the bandwidth of each VGA decreases as the number of taps connected to the common output node increases.

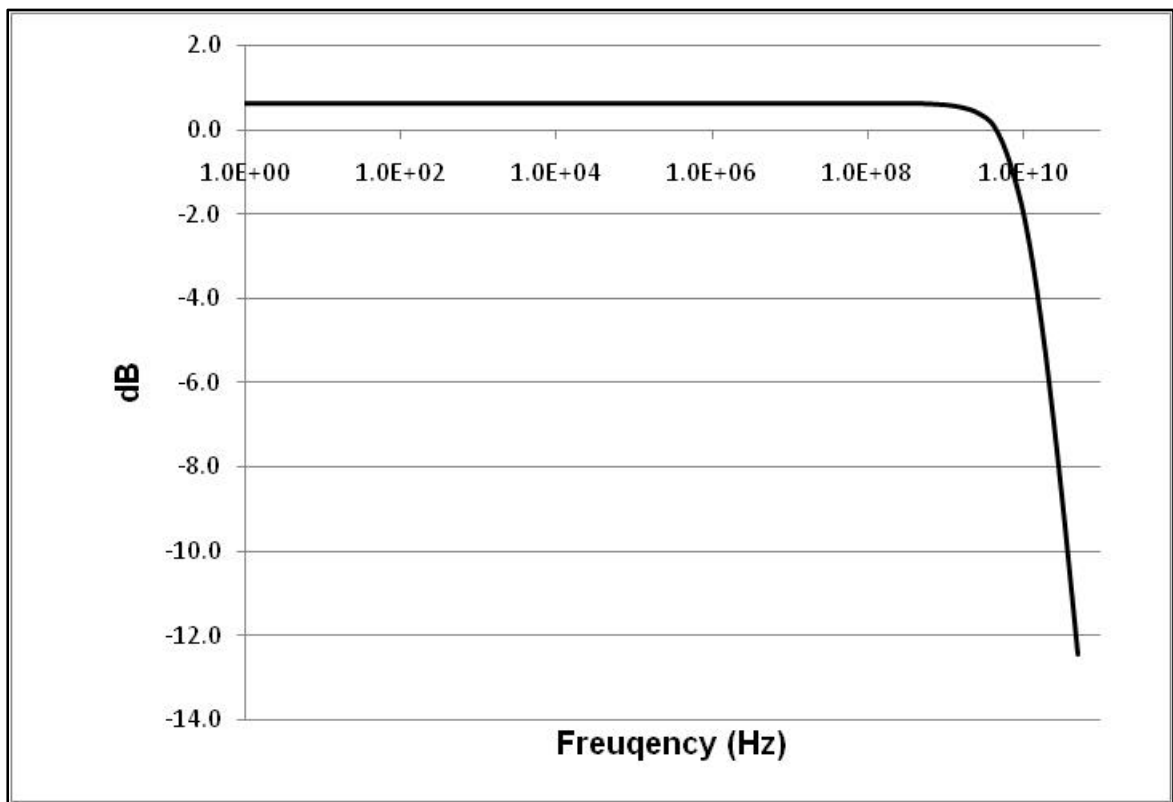


Figure 3.10 Frequency response of the VGA.

The VGA tuning circuit provides linear gain from +1.5 to -1.5 over the V_{CONT} tuning range of 0 to 1.5 V. Figure 3.11 shows the VGA gain against V_{CONT} .

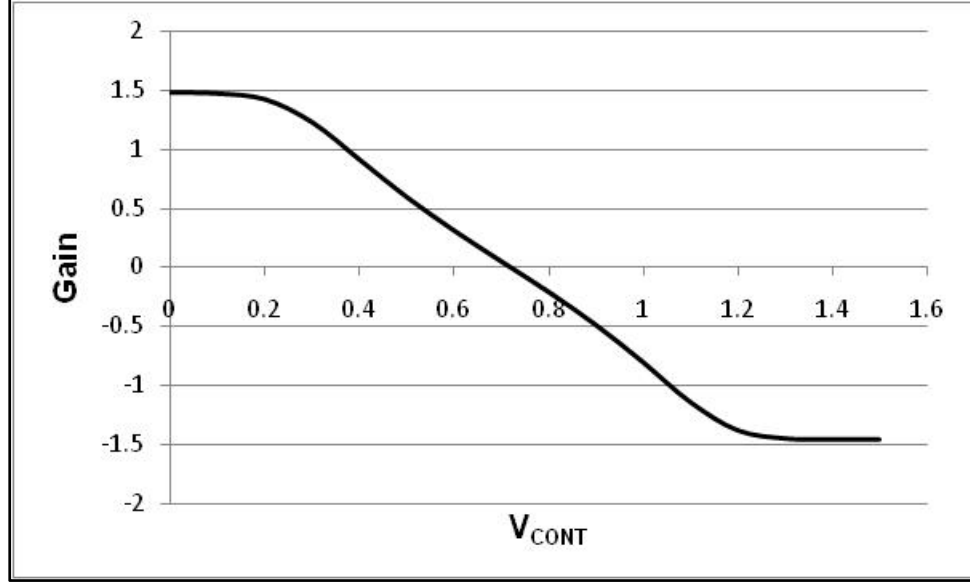


Figure 3.11 VGA gain vs. V_{CONT} .

3.3.2 Linear Active Tuneable Delay Cell

The linear active tuneable delay cell uses the RC delay from NMOS differential pairs to achieve the required delay. The delay is achieved as a result of bandwidth degradation. Figure 3.12 shows a schematic of an active delay cell. The transient delay through a NMOS differential pair, assuming linear operation, is given by (3.25). Assuming only the output pole is dominant, the $\omega_{3\text{-dB}}$ is given in (3.26).

$$t_{\text{delay}} = \frac{k}{BW} \quad (3.25)$$

$$BW = \frac{1}{2\pi RC} \quad (3.26)$$

BW is the 3-dB bandwidth of the cell in Hz. Since R and transistor size are limited in order to keep the small-signal gain equal to 1, the delay per differential pair cell is about 10-20 ps in a 0.18-um CMOS process. Previous linear filter implementations used passive LC delay lines to achieve the required delay [2.15]. The advantages of a passive delay line are improved

bandwidth compared to active implementation and lower power consumption. However, this comes with large inductor area and only fixed delay values. Furthermore, the tap delay value cannot be tuned after fabrication. For these reasons active delay cells were explored [3.8].

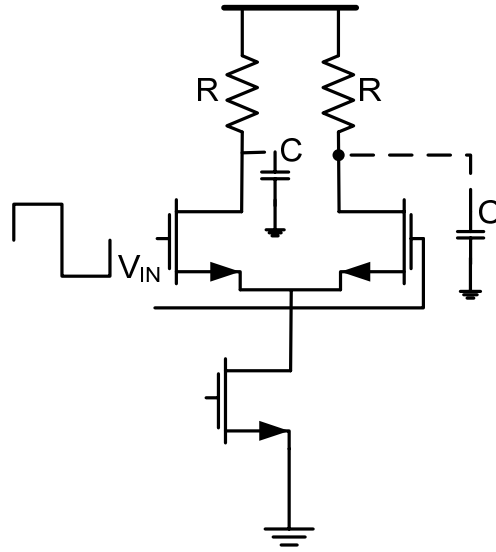


Figure 3.12 Schematic of active delay cell.

The delay value, τ , for the FFE can be $T/2$, $T/3$, $T/4$, and so on. The value of τ depends on the channel being equalized. A tuneable delay cell enables a reconfigurable FFE that can be used for a variety of channels. Furthermore, the delay value can change from its design goal over process, voltage and temperature variations. A tuneable delay feature enables dynamic tuning of the FFE during operation. A voltage-controlled tuneable delay circuit is used to achieve variable delay for a reconfigurable linear equalizer. The scheme uses a voltage-controlled current-steering mechanism to achieve different signal delays [3.8]. The design of the tuneable delay cell

is similar to the design of the delay cell used in the ADFE as is described in detail in the next chapter. The key design challenge for the FFE delay cell is minimizing parasitic elements and maximizing bandwidth per delay cell. Increasing the number of FFE taps decreases the total bandwidth of the equalizer and increases power consumption since the signal passes through an additional delay cell for each additional tap. Therefore, at 10-Gb/sec it is important to minimize the number of forward filter taps and perform additional equalization using decision-feedback equalization.

3.4 Conclusion

At multi-Gb/sec data rates, digital CMOS process is unable to keep up with the required serial data rates. Increased static and dynamic power consumption, clock feed-through, and ground bounce make implementation of traditional digital circuits to operate at 10-Gb/sec very challenging. Clock-data delay is a limiting factor in implementing the traditional digital DFE at 10-Gb/sec. CML techniques have been explored as an alternative to CMOS logic gates in several 10-Gb/sec data transmission circuits [3.6]. At 10-Gb/sec an analog FFE at the receiver has several advantages to a digital FFE at the transmitter. However, the analog FFE implementation is hindered by the headroom-bandwidth trade-off in the VGA and decreasing bandwidth as the number of taps is increased. Additional ISI cancellation can be provided using decision-feedback equalization and increasing the number of feedback taps. The next chapter will look at the design of the analog decision-feedback building blocks.

CHAPTER 4

ANALOG DECISION-FEEDBACK EQUALIZER

4.1 ADFE Building Blocks

This chapter describes the circuit building blocks of the ADFE and relevant simulation results. As discussed in Chapter 3, the primary bottleneck in implementing the conventional DFE at multi-Gb/sec data rates is the delay through the clocked decision circuit. The primary requirement for the DFE is to provide the previous symbol “decision” to the input of the decision element at multiples of the bit period. It will be shown that a rail-to-rail digital signal is not required for decision-feedback to take place [2.21, 4.1]. Furthermore, analog techniques for providing accurate signal delay can be used to make sure that the latency through each feedback loop is an exact multiple of the bit period and a clocked signal is not needed for decision-feedback to take place. The traditional topology of using a clocked decision element after the forward filter made sense when CMOS digital circuits kept pace with the data rates being processed. The decision element re-timed the data using the system clock and used the re-timed data for decision-feedback equalization. In doing so, the decision element performed the dual role of data-re-timing and equalization. However, these two functions are exclusive and can be separated. The fundamental principle behind the ADFE is the separation of decision-feedback equalization from data-re-timing. The next few sub-sections look at the building blocks of the ADFE.

4.1.1 G_M Stage

Figure 4.1 shows a block diagram of a 1-tap ADFE. The G_m block is where correction for post-cursor ISI takes place. The analog limiting amplifier (ALA) is the decision circuit. The loop latency control (LLC) circuit controls the total latency through the first feedback loop over analog variations. Figure 4.2 shows how post cursor ISI is caused in a differential data stream. A long stream of 1's is followed by a 0 and then 1's again. The roll-off of the falling edge as the transition from 1 to 0 is made is because of the band-limitation of the channel or pulse dispersion in optical fibre. The transition from 0 to 1 comes about before the signal can reach its final value. This is a missed transition due to post-cursor ISI. The previous symbols, all 1's, interfere with the 0 symbol. No detection circuit can resolve this differential signal.

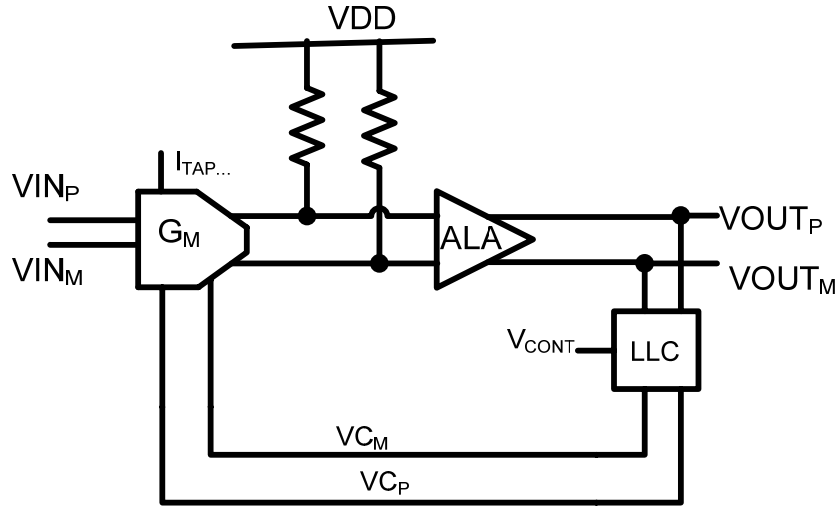


Figure 4.1 Block diagram of the ADFE.

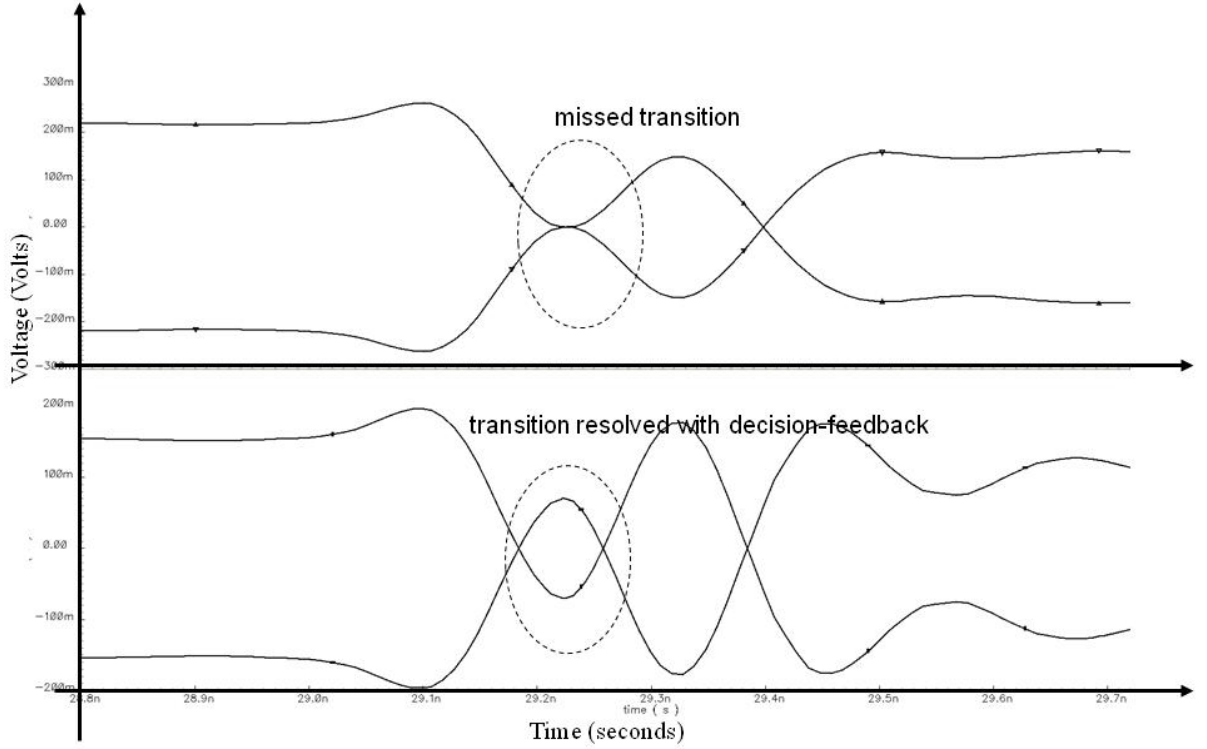


Figure 4.2 Missed transition due to post-cursor ISI [4.1].

The G_m block is where correction for the post-cursor ISI takes place and takes advantage of the differential signalling scheme used [2.21]. The input signal to the G_m block is from the output of the forward filter. Assuming that the forward filter taps are set to equalize pre-cursor ISI, the peak-to-peak voltage of the input signal could be less than 50 mV. Figure 4.3 shows a schematic of the G_m block. Transistors M1 and M2 receive the input signal V_{IN} and generate a differential current. At this stage, no gain is needed. The sizes of M1 and M2 are kept small to minimize the gate-source capacitance C_{GS} and drain source capacitance C_{DS} . C_{GS} will be part of the load capacitance seen by the forward filter. The main pole for this circuit comes from the load resistor R_L and load capacitor C_L . C_L is composed of the input

capacitance of the following stage as well as C_{DS} . Post-cursor ISI compensation takes place in the current domain. Transistors M3 and M4 are current switches controlling the first tap current I_{TAP1} . M5 and M6 are current switches controlling the second tap. There can be several pairs of switches depending on the number of taps being implemented. A 1-tap DFE is considered. The gates of M3 and M4 are controlled by the “decision” signals from the output of the first feedback loop. If the previous symbol was a 1, V_{CP} will be high and V_{CM} low. All of the I_{TAP1} is steered through M3 and through only one of the load resistors. This results in a negative shift in the DC level of the positive signal as shown in Figure 4.2. Now the difference in voltage levels between the positive and negative signal is increased and the missed transition can now be resolved by successive circuits. In this manner ISI due to more than one previous symbol can be compensated for [2.21].

The size of the current switch and the value of the load resistor determine the signal swing needed from the decision signals, V_{CP} and V_{CM} , to completely switch the tap current from one side to the other [4.1].

$$V_{decision,min} = \sqrt{\frac{2I_{TAP}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_3}} \quad (4.1)$$

I_{TAP} and R_L will determine the amount of correction, V_{CORR} , made to the signal.

$$V_{CORR} = I_{TAP} \times R_L \quad (4.2)$$

If the input signal is about 50 mV, V_{CORR} is not more than 20 mV. If R_L is set to 200 Ohms, I_{TAP} is not more than 100uA. If R_L decreases by a factor of M , the I_{TAP} needed for the same V_{CORR} increases by a factor of M . This increases the $V_{decision,min}$ needed for complete I_{TAP} switching by a factor of \sqrt{M} . This

increases the output swing requirements feedback loop by a factor of \sqrt{M} . In a 0.18- μm CMOS process, a 600 mV swing is sufficient for analog decision-feedback for the channels under consideration [4.1].

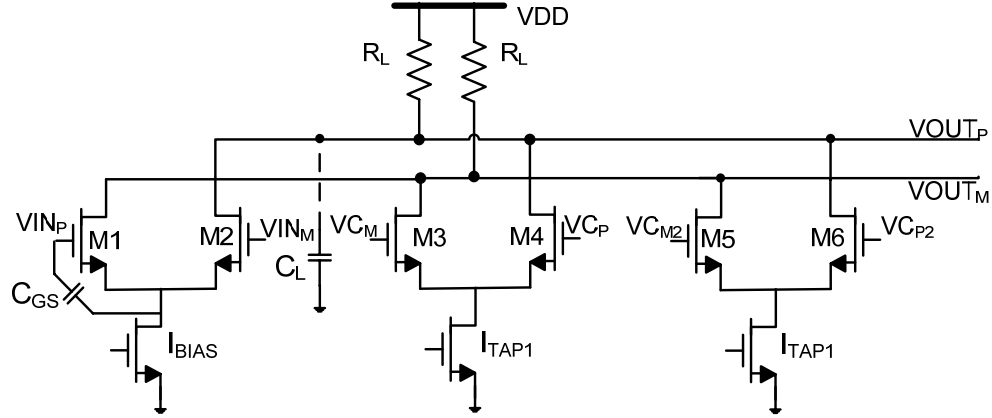


Figure 4.3 Schematic of G_m stage.

4.1.2 Analog Limiting Amplifier (ALA)

The clocked decision circuit is the primary bottleneck in implementing a digital DFE at multi-Gb/sec data rates. Specifically, the clock-data delay of a clocked comparator consumes a significant portion of the first feedback loop timing budget, making the traditional topology challenging or unfeasible. The previous section illustrated how correction for post-cursor ISI takes place in the analog domain. The G_m stage needs decision signals with a 600 mV swing. Rail-to-rail signals are not needed. An unclocked limiting amplifier that can amplify the small analog signal after the G_m stage can perform this function. The design challenge for the ALA is to achieve the necessary small signal gain and large signal swing as well as maintain bandwidth for a 10-Gb/sec NRZ signal and keep the latency through the circuit less than 100 ps. The rest of this section will illustrate how these goals are met.

Cascading several gain cells is a technique that has been used to achieve gain and maintain bandwidth in multi-Gb/sec limiting amplifiers [4.3]. If latency was not a design goal, several gain cells can be cascaded to achieve the required gain and bandwidth in a 0.18-um CMOS process. A differential pair with resistive loads as shown in Figure 4.4 can be considered as a baseband amplifier to provide large output swing. Cascading several such identical cells would provide an output swing as given in (4.3).

$$V_{SWING} = V_{DD} - I_{BIAS} \times R_{LOAD} \quad (4.3)$$

The number of cascaded cells would determine the sensitivity of the limiting amplifier. The first few cells would operate in small-signal mode with a small signal gain of A_v . However, as the input signal gets larger, the differential pair behaves as a limiting amplifier.

$$A_v = -g_m \times R_{LOAD} \quad (4.4)$$

$$V_{min} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \quad (4.5)$$

When the input signal of a differential stage is $\geq V_{min}$, the differential pair operates in large-signal mode and completely switches the bias current I_{SS} to one side. The circuit is now limiting in action and the output signal levels are limited to V_{DD} and V_{SWING} even as the input signal gets larger.

The 3-dB bandwidth of each gain cell is determined by the load resistor, R_{LOAD} and the load capacitor C_{LOAD} . C_{LOAD} is composed mainly of the gate-source capacitance C_{GS} of the next stage. However, additional capacitances are also present due to the Miller effect [4.4]. Assuming identical device sizes, finite bulk-source voltage, $R_{LOAD} \ll r_{ds}$, and ac ground at the common-source node, the small-signal DC gain is given by (4.6). C_{LOAD} is given as in (4.7).

$$A_v = -(g_m + g_{mbs}) \times R_{LOAD} \quad (4.6)$$

$$C_{LOAD} = C_{GS} + C_{GD}(1 + A_v) + C_{GD}((A_v + 1)/A_v) + C_{DB} \quad (4.7)$$

The first term on the right-hand side of (4.7) is the gate-source capacitance of the loading transistor. The second term is the input Miller capacitance of the loading cell. The third term is the output Miller capacitance of the primary transistor and the last term is the drain-bulk capacitance of the primary transistor. So, increasing the gain of the transistor by increasing g_m or R_{LOAD} also increases the total effective load capacitance at the output node, which decreases the bandwidth and increases latency through the circuit.

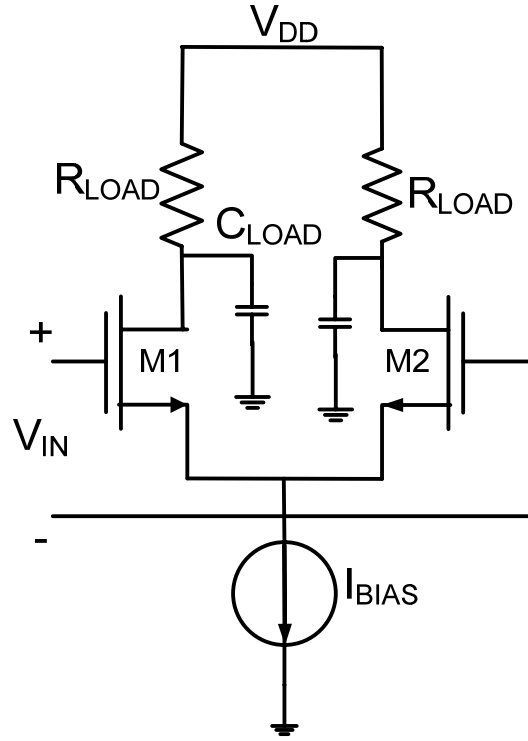


Figure 4.4 Schematic of differential pair baseband limiting amplifier.

Furthermore, cascading several identical gain cells also causes the poles of each stage to overlap and reduce the total bandwidth [4.3].

$$BW_{TOT} = BW_C \sqrt[m]{2^n - 1} \quad (4.8)$$

where $m=2$ for first-order cell and 4 for second order cells. Also, for a total gain of A_{TOTAL} , the cell gain-bandwidth GBW_C can be defined as in (4.9).

$$GBW_C = \frac{GBW_{TOTAL}}{A_{TOTAL}^{1-\frac{1}{n}} \sqrt[m]{\frac{1}{2^n}-1}} \quad (4.9)$$

So the design goal for the ALA is maximize the GBW of each stage and minimize the number of cascaded stages.

This work uses a 2-cell ALA. Each cell consists of 2 stages of gain. Active negative feedback is utilized to maximize the GBW of each cell [4.3]. Figure 4.5 shows a block diagram of the scheme used in each cell. A transconductance stage, G_{mf} , is used to return a fraction of the output to the input of G_{m2} . This is a modification of a traditional Cherry-Hooper amplifier. However, unlike the traditional Cherry-Hooper amplifier, which uses resistive feedback, the active feedback does not resistively load the transimpedance stage [4.3]. Figure 4.6 shows a schematic of the cell used. The primary design variables are (W/L) of the transistors, tail current, $I_{BIAS1,2,3}$ and load resistor, R_{LOAD} .

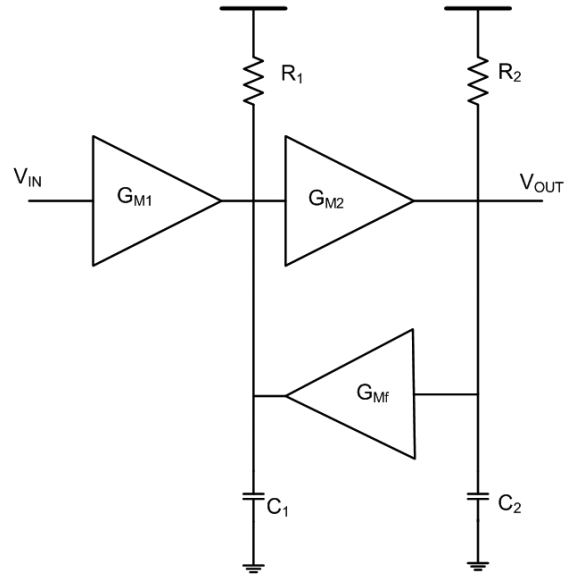


Figure 4.5 Block diagram of active negative feedback.

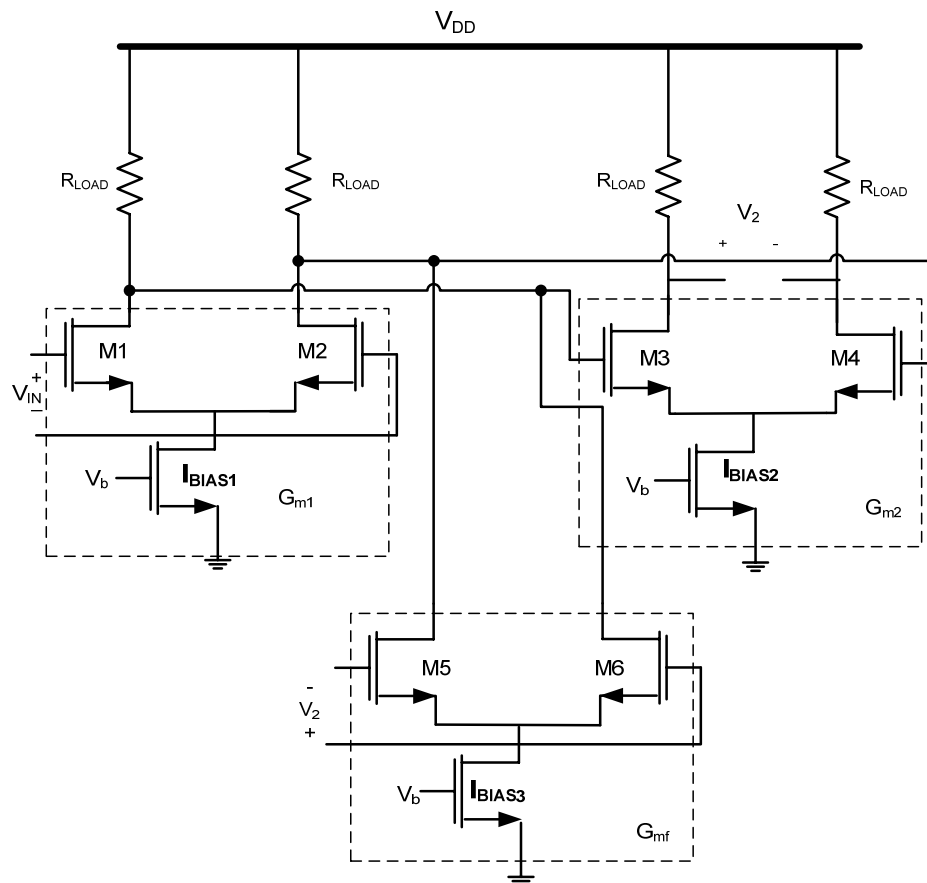


Figure 4.6 Schematic of one ALA cell [2.21].

The transfer function of the cell is given by (4.10) [4.3].

$$\frac{V_{out}}{V_{in}} = \frac{A_v \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \quad (4.10)$$

$$A_v = \frac{G_{M1} G_{M2} R_1 R_2}{1 + G_{M2} G_{MF} R_1 R_2} \quad (4.11)$$

$$\zeta = \frac{1}{2} \left(\frac{R_1 C_1 + R_2 C_2}{\sqrt{R_1 C_1 R_2 C_2} \sqrt{1 + G_{M2} G_{MF} R_1 R_2}} \right) \quad (4.12)$$

$$\omega_n^2 = \frac{1 + G_{M2} G_{MF} R_1 R_2}{R_1 C_1 R_2 C_2} \quad (4.13)$$

From [4.3] we have the following results:

$$A_v \omega_{3-db}^2 = \frac{G_{M1} G_{M2}}{C_1 C_2} \quad (4.14)$$

$$A_v \omega_{3-db} = \frac{G_{M1} G_{M2}}{C_1 C_2} \frac{1}{\omega_{3-db}} \quad (4.15)$$

Since $G_{M1}/C_1 \cong G_{M2}/C_2 = 2\pi f_T$,

$$A_v \omega_{3-db} = f_T \frac{f_T}{f_{3-db}} \quad (4.16)$$

This result shows that active negative feedback increases the cell bandwidth beyond the technology f_T by a factor equal to the ratio of the f_T to the cell bandwidth [4.3]. The frequency response of the ALA cell is shown in Figure 4.7. Each cell has a DC gain of 7.5 dB and a 3-dB bandwidth of 16 GHz. The complete ALA consists of 2 identical cascaded cells.

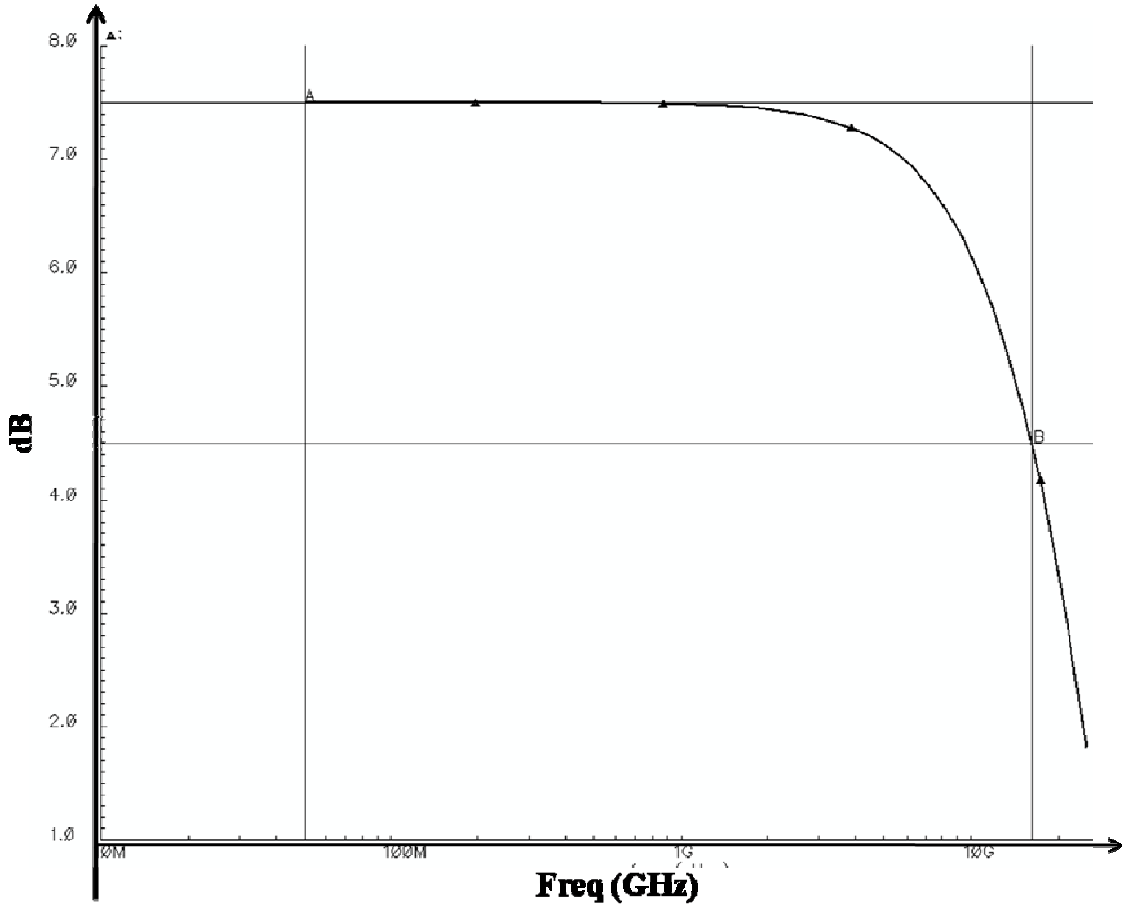


Figure 4.7 Frequency response of one ALA cell

4.1.3 Loop Latency Control (LLC)

The latency through the ALA can vary with process, voltage and temperature. The resistor values vary about 15 % with from slow to fast process. In addition supply voltage variations and temperature fluctuations can cause a deviation in the ALA latency from the design goal. The circuit requires some external control over the latency of the first feedback loop. The LLC circuit consists of cascading CML cells such that the V_{min} of each cell is $\geq V_{out}$. The delay through each cell is due to the RC delay of each cell. Variable

delay is achieved by using a voltage-controlled current-steering scheme that creates a dominant and a non-dominant signal path [3.8]. Figure 4.8 shows a functional representation of this mechanism. V_{CONT} is the control voltage in the final tuning cell. A slow signal path exists between V_{IN} and V_{OUT} through cells 1, 2, 3, and 4. A fast signal path exists from V_{IN} to V_{OUT} through cell 4 only. When V_{CONT} is at the low value of its operating range, the fast signal path is activated and the input signal goes through cell 4 to the output. When V_{CONT} is at the maximum value of its operating range, the slow signal path is activated and the input signal travels through cells 1, 2, 3, and 4. For in-between values of V_{CONT} , a range of signal transit times are obtained.

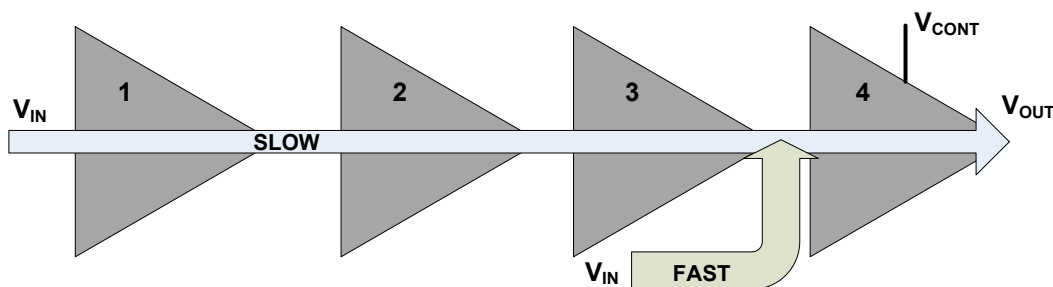


Figure 4.8 Function representation of LLC circuit.

Figure 4.9 shows a simplified schematic of the tuning cell 4. V_{REF} , the reference voltage is set to 720 mV using a series resistor chain. V_{IN} is the primary input and V_X is the output after 3 LLC cells. Each LLC cell consists of a NMOS CML differential pair with resistive loads as described in Chapter 3. The delay through each LLC cell is a result of the RC load of each cell. V_{IN} denotes the fast signal path input and V_X denotes the slow signal path input. V_{CONT} controls the flow of the bias current I_{CONTROL} through the PMOS switches M13 and M14. When V_{CONT} is at the low end of its operating range

with respect to V_{REF} , M13 turns on and all the control current flows into the diode M11 and then mirrored over to M10. The bias current in M9 is almost zero. Only transistors M7 and M8 are biased and the fast signal path of V_{IN} to V_{OUT} is activated. When V_{CONT} is at the high end of its operating range with respect to V_{REF} , M14 turns on and all the control current flows into the diode M12 and then mirrored over to M9. The bias current in M10 now is almost zero. Only transistors M5 and M6 are biased and the slow signal path of V_X to V_{OUT} is activated. For in-between values of V_{CONT} , varying signal delay is achieved. The upper limit of the range of delay is determined by the number of LLC cells and the lower limit is determined by which LLC cell output is connected to the V_X input of the final cell. Figure 4.10 shows the tuning range of the LLC circuit as a function of V_{CONT} [2.21].

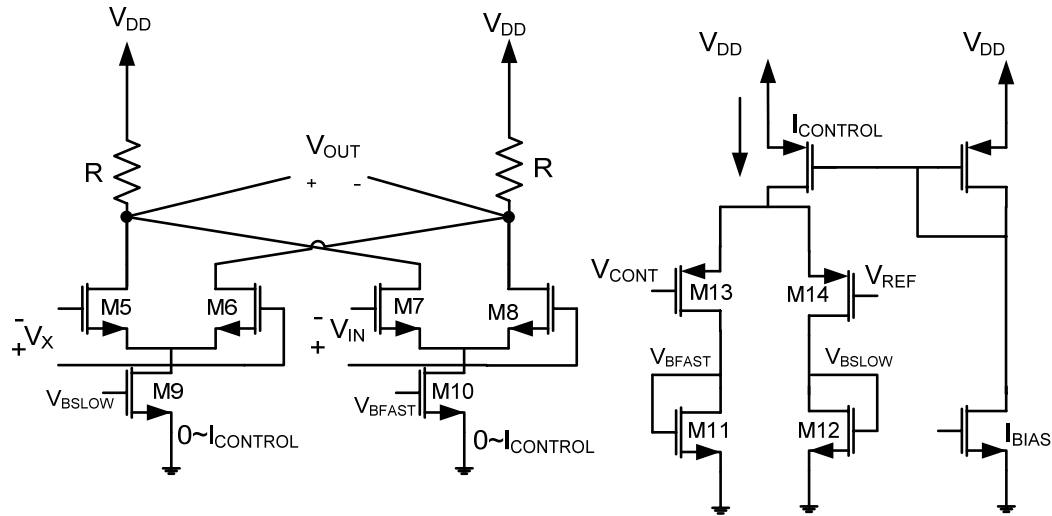


Figure 4.9 Schematic of tuning cell [2.21].

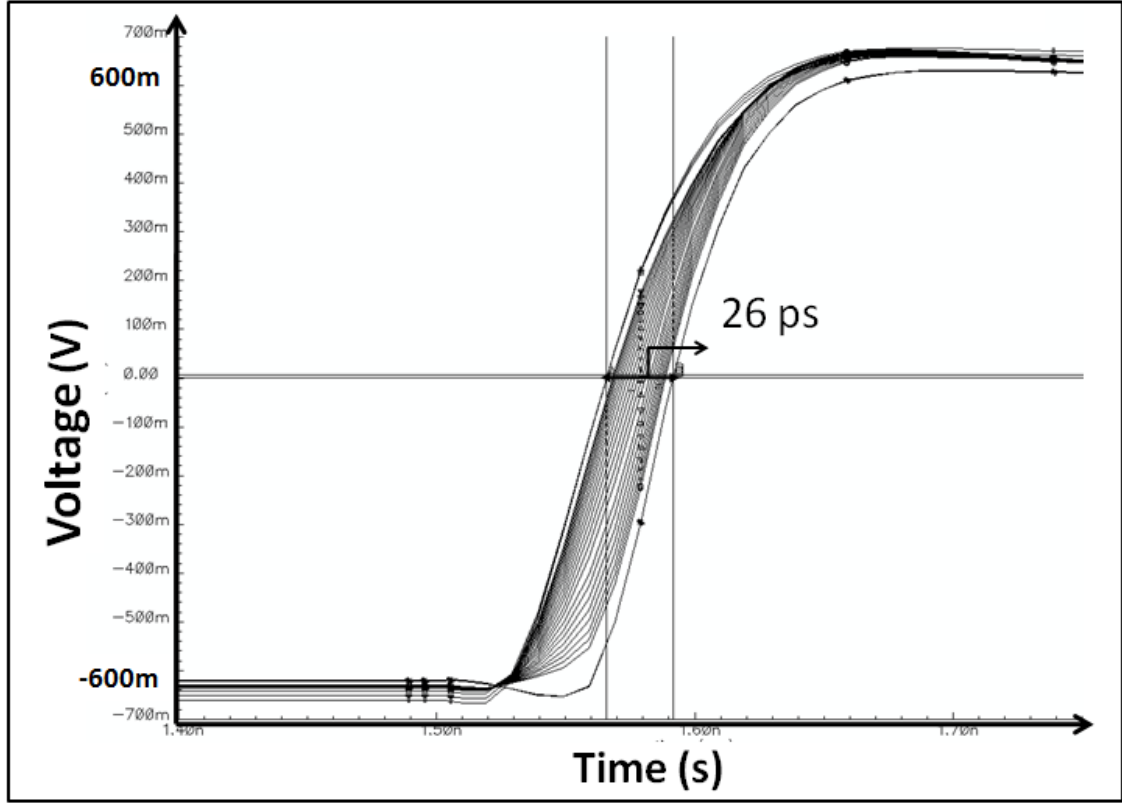


Figure 4.10 Tuning range of LLC circuit [4.3].

4.2 Layout Techniques

Physical layout of the circuit is a critical element in multi-Gb/sec IC design. A number of techniques were used to minimize the effects of parasitic capacitances and resistances, as well as device mismatch. The layout and orientation of the devices is critical to maintain perfectly differential signal path from the input to the output of the circuit. This is particularly challenging given the feedback loops within the ADFE circuit. The following sections briefly describe some of the important layout techniques used to achieve optimum performance.

4.2.1 Resistor Layout

The ADFE uses passive resistors extensively for high-speed operation and to achieve the wide signal swing required for CML operation. TSMC layout design guide states that N_{sq} for poly resistors must be ≥ 2 . This means that to implement a 1.2kOhm resistor requires four 300-Ohm resistors in parallel. For differential pairs it is very important that the resistor value on both legs is exactly the same. Difference in resistor values could give rise to voltage offsets that could be amplified considerably down the signal path resulting in a large DC offset at the output. Therefore, dummy poly or resistors are used on either side of the bank of poly resistors to minimize the effect of random mismatches in the width of the poly caused by the etching process for different resistors of the same value. Figure 4.11 shows a picture of the resistor layout with the dummy resistors surrounding the device resistors.

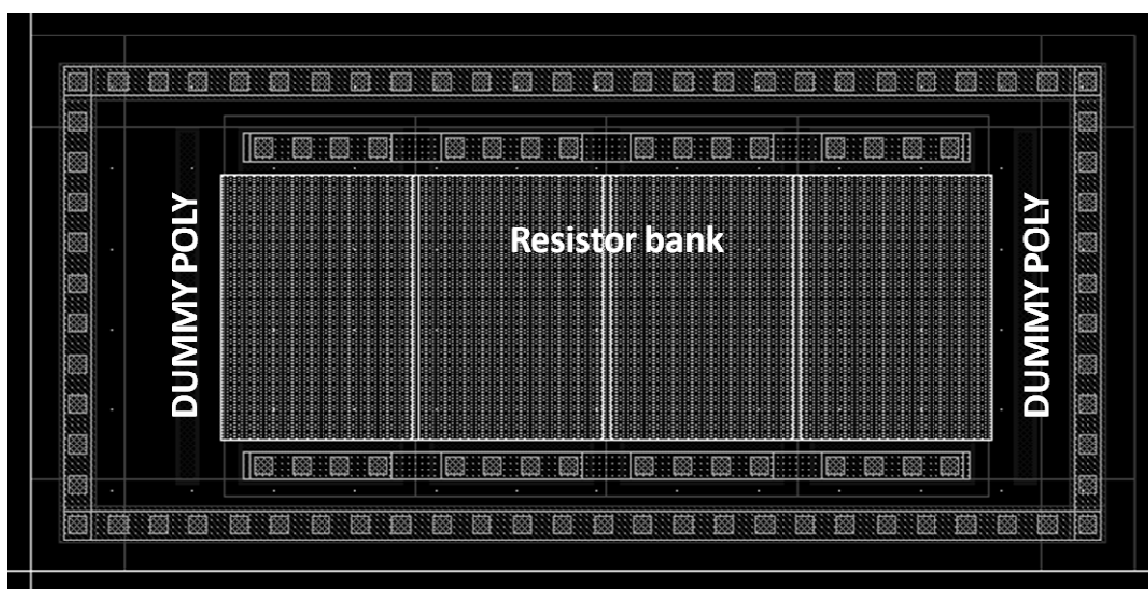


Figure 4.11 Resistor bank with dummy poly on sides.

4.2.2 Transistor Layout

Similarly, dummy fingers with the same width as the input devices were placed to either side of the input devices to minimize mismatch caused by poly etching. A mismatch at any stage of the ADFE could cause a DC offset at the output of a differential pair stage resulting in a huge offset at the chip output due to the high gain in the signal path. In addition the differential pairs were interdigitated. The number of fingers was kept even wherever possible and attempts were made to keep the shape of the transistors square. The number of contacts and vias were decreased in order to minimize parasitic capacitances, while meeting current density specifications. The orientation of all input transistors were kept the same so that cascading stages could abut easily to each other, thereby minimizing mismatch and shortening the signal path.

4.2.3 Symmetric layout for differential signal paths

Since the ADFE makes use of differential signalling to cancel the post cursor, keeping the differential signal paths of equal length throughout the circuit is very important. Symmetry also ensures equal parasitic on both signals. Figure 4.12 shows a layout of a CML cell. The input NMOS devices are at the centre. The load resistors are above and below the transistors to ensure equal length from the drain contact to the resistor. The source transistor is placed below the resistor. The V_{DD} node forms a bus around the entire input pair core to minimize parasitic resistance on either leg. The width of the bus is kept large for the same reason. Extensive substrate

contacts are used around each differential pair and resistors to minimize the path to circuit ground.

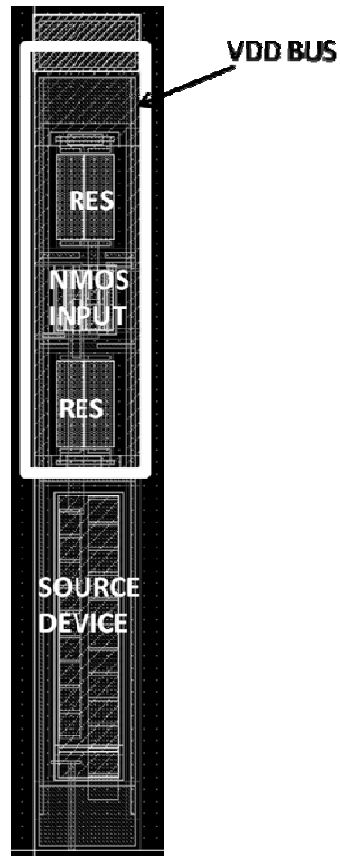


Figure 4.12 Layout of CML cell.

CHAPTER 5

MEASUREMENT RESULTS

This chapter illustrates the measurement results of the ADFE. Two circuits were fabricated in TSMC's 0.18-um CMOS process and measured using on-wafer probing techniques. The first circuit, C1, consists of a 4-tap forward filter and a 1-tap feedback filter. The second circuit, C2, consists of a 2-tap forward filter and a 2-tap feedback filter and is fabricated to illustrate that the ADFE concept can be extended to a multi-tap feedback architecture without resulting in instability. The circuits are used to equalize FR-4 backplane, MMF and SMF at 10-Gb/sec.

Figures 5.1 and 5.2 show die photographs of C1 and C2. Table 5.1 lists the specifications of C1 and C2. In both circuits, the forward equalizer tap coefficients are controlled using V_{C0n} and the tap delay with V_{FFE} . The feedback equalizer tap coefficients are controlled using I_{TAPn} and the feedback equalizer loop delay with V_{CONT} in C1 and V_{DFE_1} and V_{DFE_2} in C2. When I_{TAPn} is turned off, the output is the effect of just the linear forward equalizer and the output driver. When I_{TAPn} is turned on the effect of analog decision-feedback can be seen. The following sections look at backplane and MMF equalization using C1 and C2.

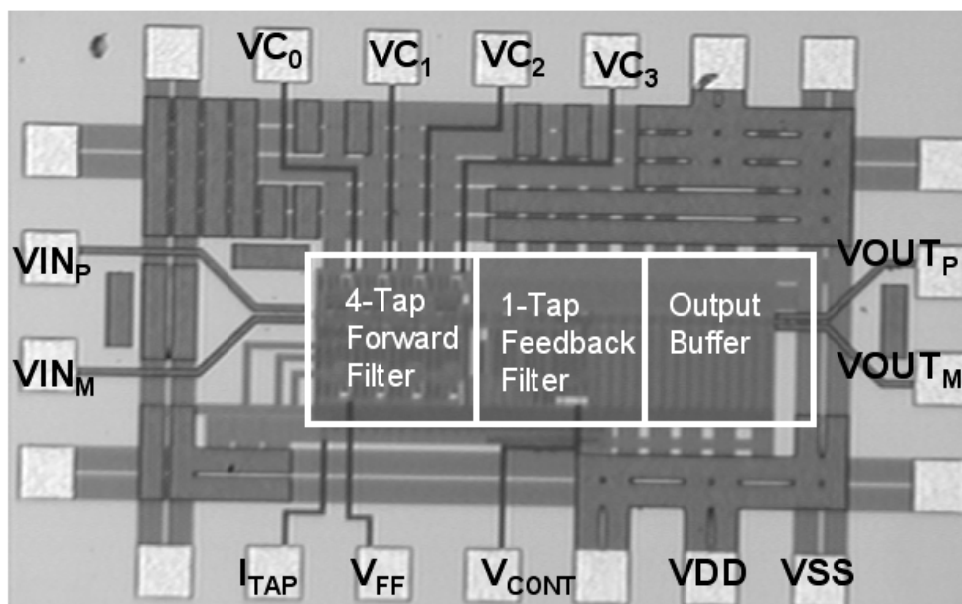


Figure 5.1 Die photo of ADFE with 4 FFT and 1 FBT [2.21].

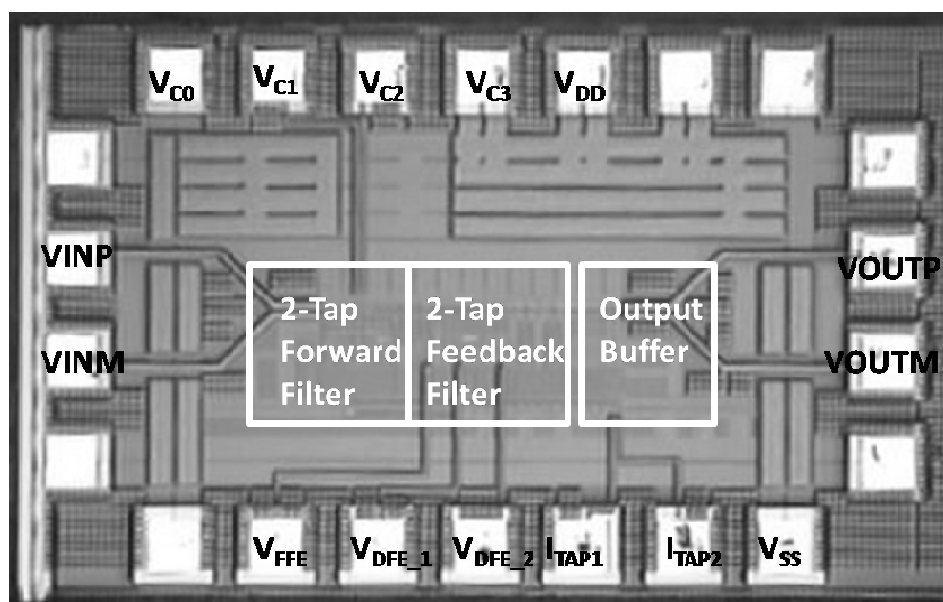


Figure 5.2 Die photo of ADFE with 2 FFT and 2 FBT.

Table 5.1 Specifications of C1 and C2.

Parameters	C1	C2
No. of forward taps	4	2
No. of feedback taps	2	2
DC current consumption	240 mA	130 mA

5.1 Backplane Equalization

Figure 5.3 shows a block diagram of the test set-up. The input differential signal is generated using Agilent's PRBS pattern generator. The signal is fed to a Tyco backplane channel daughter card. The output from the receiver side daughter card is sent to the input of C1. The output of the ADFE is looked at using an oscilloscope. Alternatively, the output can be sent to the error detector to measure BER. The eye-diagram is used to qualitatively look at the effect of analog decision-feedback and evaluate the circuit performance.

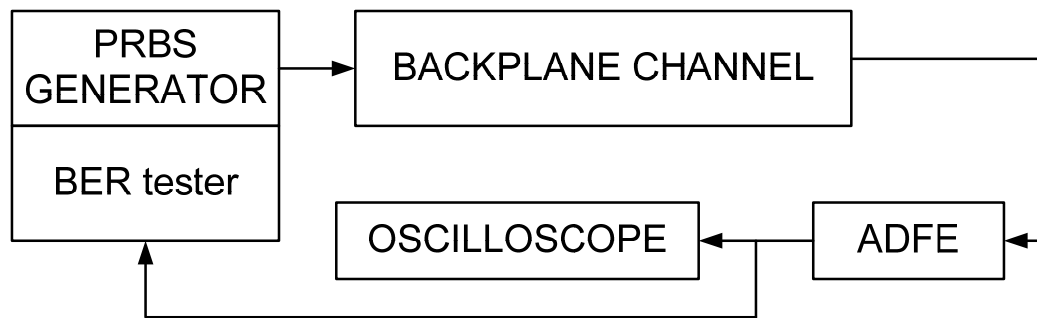
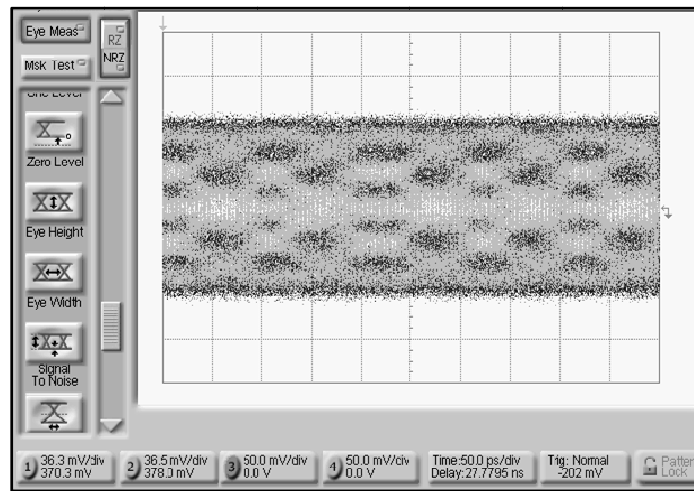


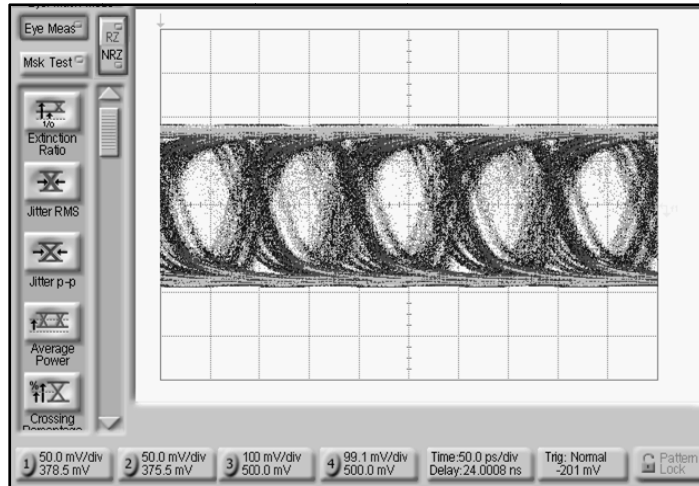
Figure 5.3 Block diagram of measurement set-up.

Figure 5.4 (a) shows the eye-diagram of a 10-Gb/sec PRBS $2^{23}-1$ signal after a 6-inch Tyco backplane channel. The eye is completely closed due to ISI caused by high-frequency channel loss. This signal is then applied to the input of the C1 ADFE circuit. Figure 5.4 (b) shows the eye-diagram of the ADFE output signal with the feedback tap turned off. This represents the effect of just the linear feed-forward equalizer. The signal passes through the forward filter, the ALA and the output buffer. However, since I_{TAP} is off, no decision-feedback is taking place. Figure 5.4 (c) shows the eye-diagram of the ADFE output signal with I_{TAP} turned on. When the tap current is turned on, post-cursor ISI correction takes place in the G_m block. The eye is clearly more open in 5.4(c) and shows improved performance with analog decision-feedback. The performance of the ADFE can be evaluated qualitatively by analyzing the improvement in the eye-diagram of the output signal.

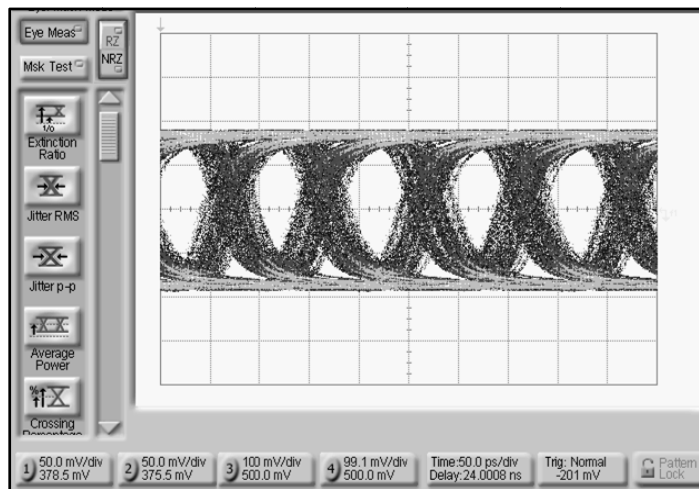


(a)

Figure 5.4 Eye-diagram of a 10-Gb/sec PRBS $2^{23}-1$ signal after (a) 6-inch FR-4 Tyco backplane channel (b) After ADFE with I_{TAP} off and (c) After ADFE with I_{TAP} on [5.1].



(b)



(c)

Figure 5.4 continued.

BER is a more quantitative measure of receiver performance. Figure 5.5 shows the BER performance for the same channel. The BER improves from $> 10^{-1}$ when the feedback tap is turned off, to $< 10^{-7}$ when the feedback tap is turned on. The improvement in BER when the feedback tap is turned on demonstrates the performance improvement with decision-feedback and also proves the concept of the novel analog decision-feedback equalization technique.

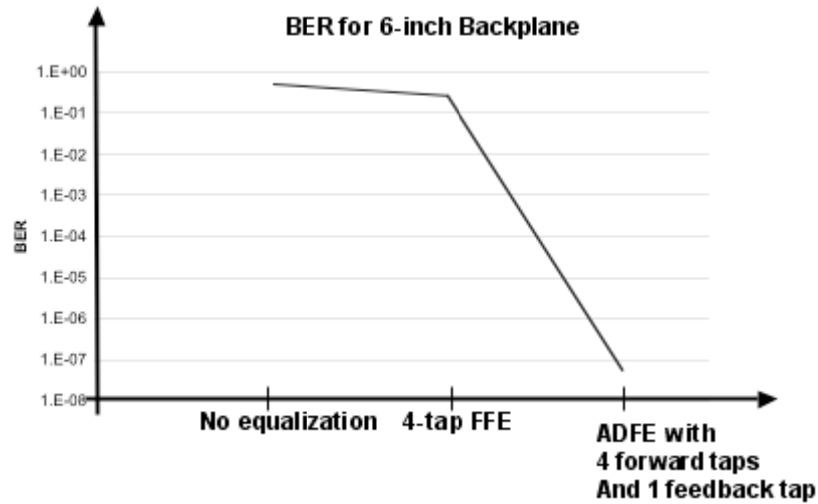
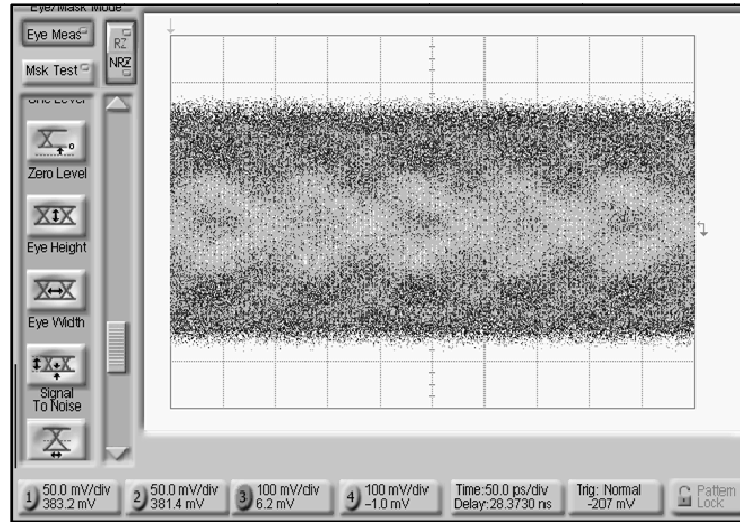
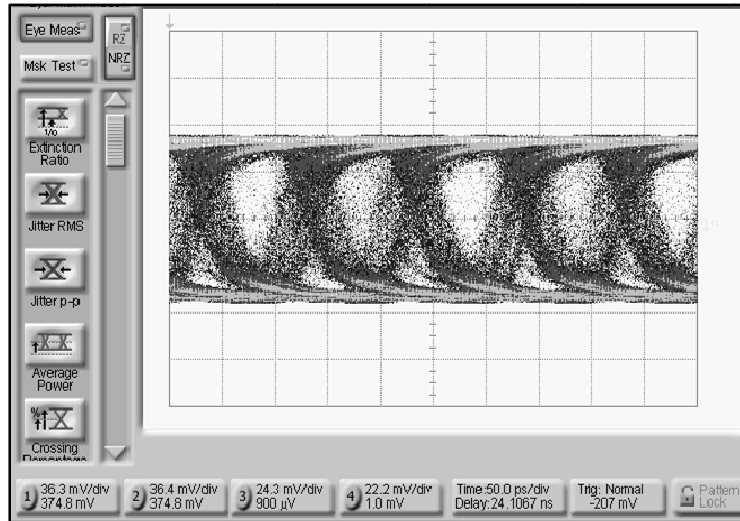


Figure 5.5 BER for 6-inch backplane [5.1].

Similar measurements were done for a 20-inch Tyco FR-4 backplane. Figure 5.6(a) shows the eye-diagram of a 10-Gb/sec PRBS signal after a 20-inch Tyco FR-4 backplane channel. The eye is completely closed. This signal is fed to the ADFE input and the eye-diagram of the output signal is measured using the oscilloscope. Figure 5.6(b) shows the eye-diagram with the feedback tap turned off and Figure 5.6(c) shows the eye-diagram with the feedback tap turned on. Although the eye still exhibits jitter, the eye is more open with feedback tap on, demonstrating the performance improvement with analog decision-feedback.

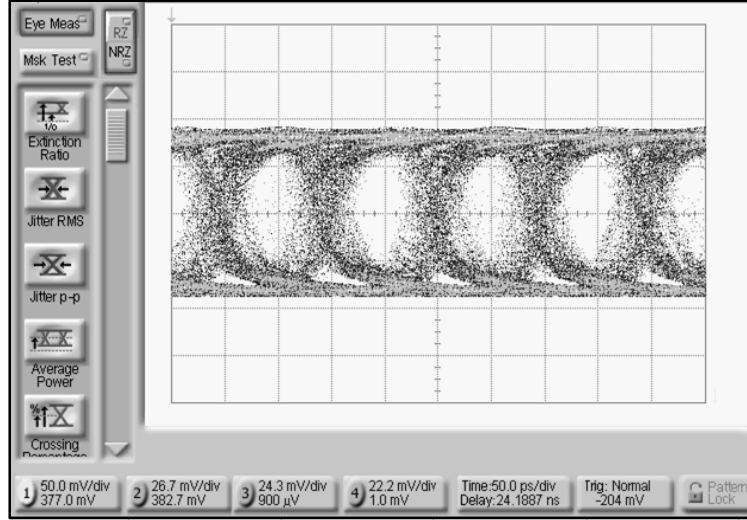


(a)



(b)

Figure 5.6 Eye-diagram of 10-Gb/sec PRBS $2^{23}-1$ data after (a) 20-inch FR-4 backplane channel (b) After ADFE with I_{TAP} off and (c) After ADFE with I_{TAP} on [4.2].

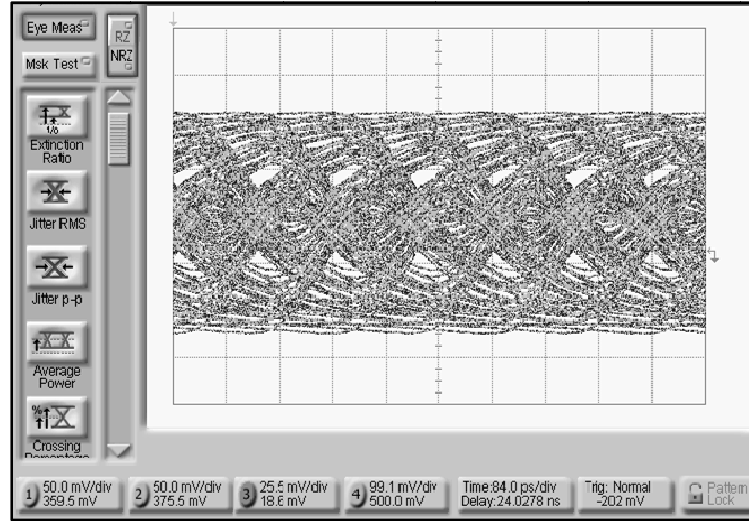


(c)

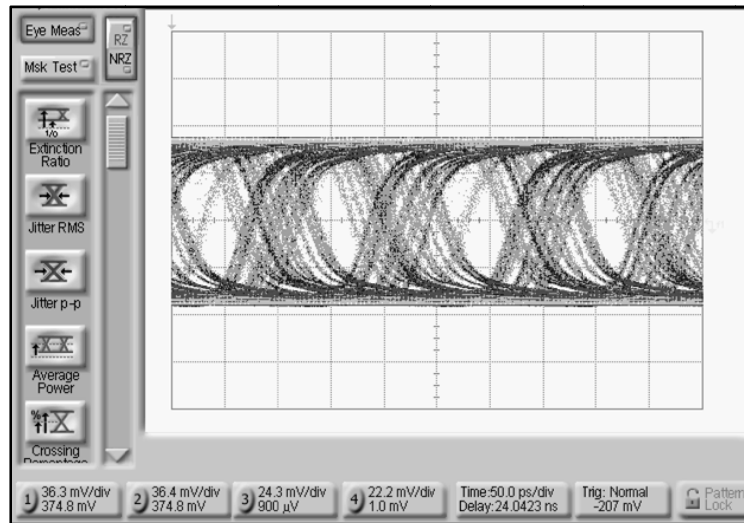
Figure 5.6 continued.

Since the feedback loop delay is tuneable, the ADFE can operate for a range of data rates. For 8-Gb/sec, the T_{sym} is 125 ps. The feedback loop LLC has the required range and can equalize an 8-Gb/sec data rate signal as well. Figure 5.7 (a) shows the eye-diagram of 8-Gb/sec PRBS data through a 20-inch FR-4 backplane channel. The eye is closed and equalization is required. Figure 5.7(b) shows the output signal after the ADFE with the feedback tap off and Figure 5.7(c) shows the output signal after the ADFE with the feedback tap on. The improvement in the eye-diagram with decision-feedback can be seen and evaluated qualitatively. Figure 5.8 shows the performance at 8-Gb/sec of the ADFE with the 2-tap forward filter and 2-tap feedback filter. The BER in both cases improves from greater than 10^{-1} before equalization to less than 10^{-7} after equalization. The second feedback tap does not induce instability but does not enhance performance either compared to the circuit with one feedback tap. For this particular channel, reducing the number of

feed-forward taps and increasing the number of feedback taps does not improve performance.

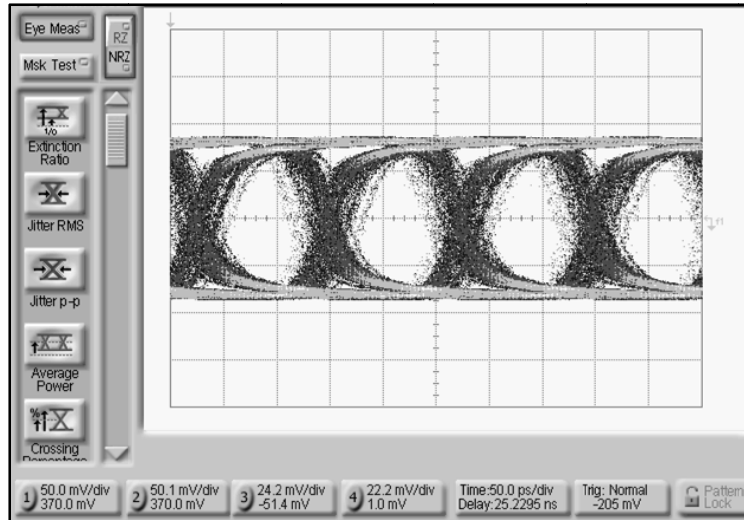


(a)



(b)

Figure 5.7 Eye-diagram of 8-Gb/sec PRBS $2^{23}-1$ after (a) 20-inch FR-4 backplane channel (b) After ADFE with I_{TAP} off and (c) After ADFE with I_{TAP} on.



(c)

Figure 5.7 continued.

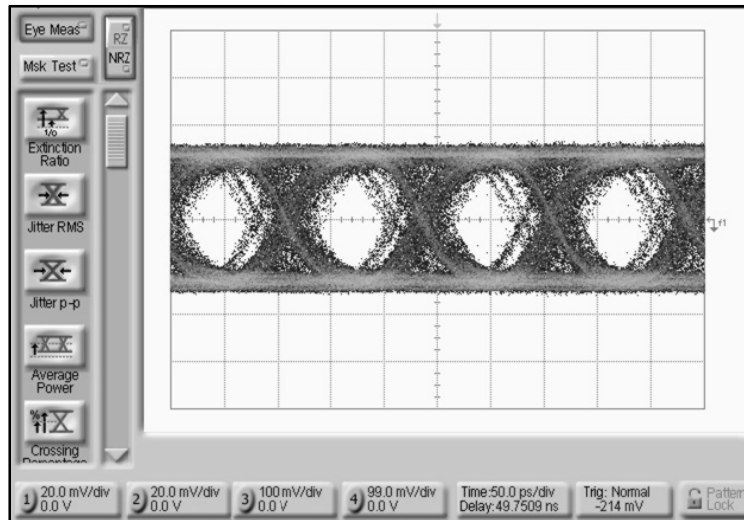
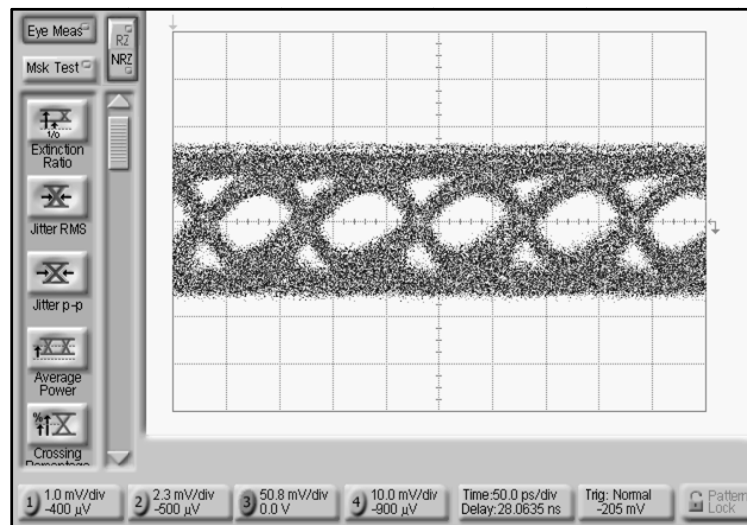


Figure 5.8 8-Gb/sec 20-inch FR-4 performance after C2.

5.2 MMF Dispersion Compensation

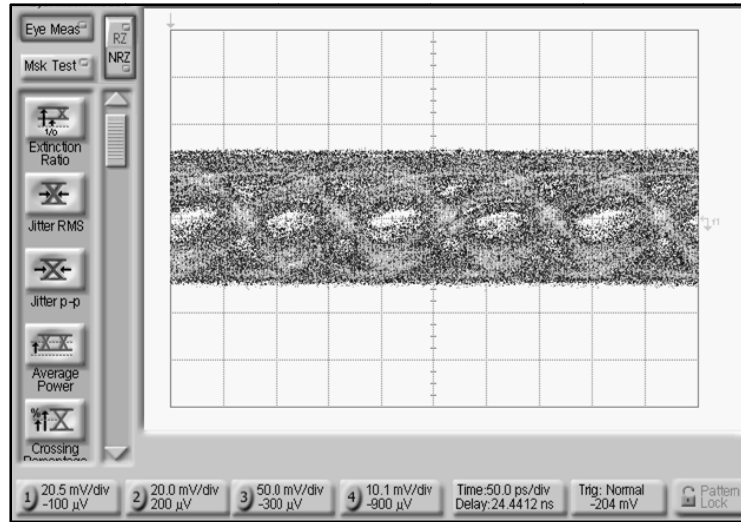
The ADFE was used to compensate for DMD in MMF at 10-Gb/sec. The PG modulates a New Focus VCSEL. The modulated light travels through 300 m MMF and is received using a New Focus photodetector. A balun is used to

drive the differential input of the ADFE with the single-ended output of the photoreceiver. The output of the ADFE is analyzed using the oscilloscope. Figure 5.9(a) shows the eye-diagram of a 10-Gb/sec PRBS $2^{23}-1$ signal after a 100 m MMF cable and Figure 5.9(b) shows the eye-diagram after a 300 m MMF cable. The effect of DMD is significantly more at 300 m. The effect of the balun is also included. C1 is used to equalize the signal after 300m of MMF. The signal after 300 m MMF is fed to the input of C1. Figures 5.10 (a) and (b) then show the eye-diagram of the output signal after the ADFE with and without analog decision-feedback. The results show that analog feed-forward and decision-feedback equalization can successfully compensate for modal dispersion in MMF at 10-Gb/sec [2.21].



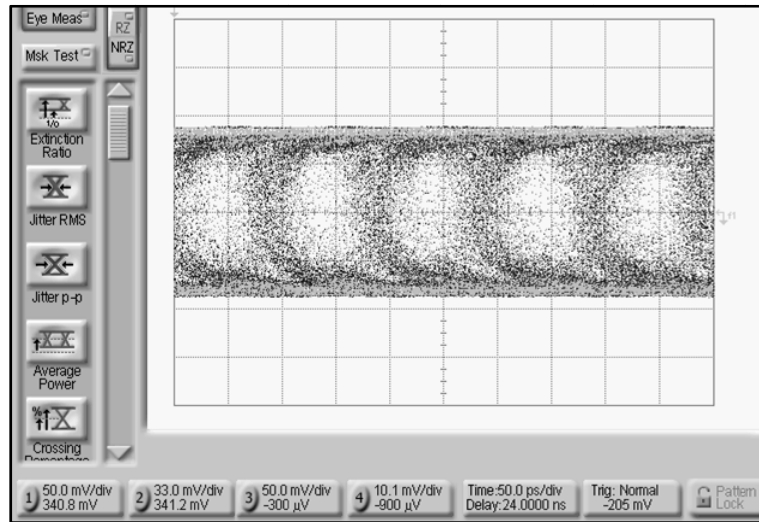
(a)

Figure 5.9 Eye-diagram of 10-Gb/sec PRBS $2^{23}-1$ (a) After 100 m MMF. (b) After 300 m MMF [2.21].



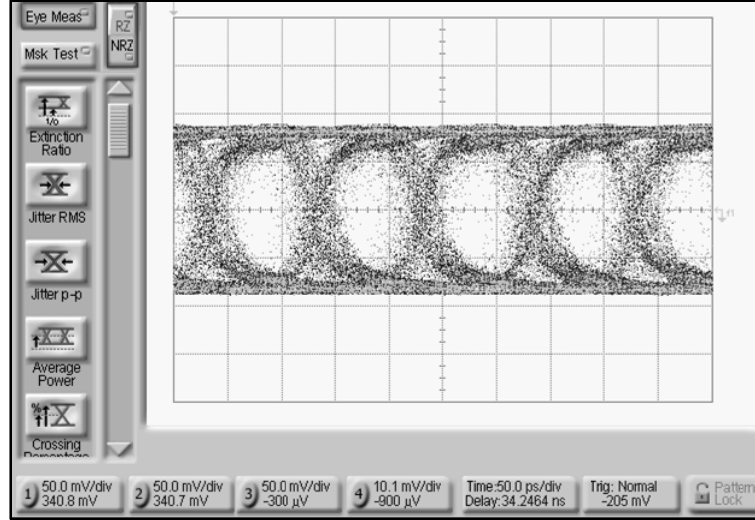
(b)

Figure 5.9 continued.



(a)

Figure 5.10 Eye-diagram of output signal (a) after ADFE with I_{TAP} off and (b) After ADFE with I_{TAP} on [2.21].



(b)

Figure 5.10 continued.

5.3 SMF Compensation

The ADFE is also applied to the output of SMF to extend the transmission distance at 10-Gb/sec. OptiSystem, a commercial optical systems simulation tool is used to simulate a 10-Gb/sec point-to-point optical link. Table 5.2 illustrates the simulation parameters. The fibre length is varied between 80 km and 140 km resulting in total chromatic dispersion between 1360 ps/nm and 2380 ps/nm [4.3]. Higher order dispersion, PMD and fibre nonlinearities are not included in the simulation. Laser noise contributions are not included in the simulation.

Table 5.2 SMF simulation parameters.

Dispersion factor	17 ps/km/nm
Wavelength	1550 nm
Modulator	Zero-chirp external Lithium Niobate
Modulator extinction ratio	30 dB
Optical SNR (OSNR)	18 dB at fibre output
Receiver responsivity	1 A/W
Receiver noise	10^{24} W/Hz

Figure 5.11(a)-(d) shows the eye-diagram of a 10-Gb/sec signal after 80 km, 100 km, 120 km and 140 km of SMF. The dotted lines indicate the eye centre or threshold. The eye-diagram shows asymmetric noise variance on the 1's and 0's. Chromatic dispersion effects and amplifier noise result in eye closure at 120 km. The signal after 120 km is applied to C1. Figure 5.12 (b) shows the clean eye-diagram at the output of the ADFE when the feedback tap current, I_{TAP} is turned on. Furthermore, the bit errors at the output of the ADFE are monitored by comparing to the input data stream. The error rate improves from 0.046 ($>BER \cong 10^{-2}$) when the feedback tap is turned off to 0 ($<BER \cong 10^{-15}$) when the feedback tap is turned on. Once again, this validates the feasibility of the analog decision-feedback topology and circuit architecture at 10-Gb/sec [4.3].

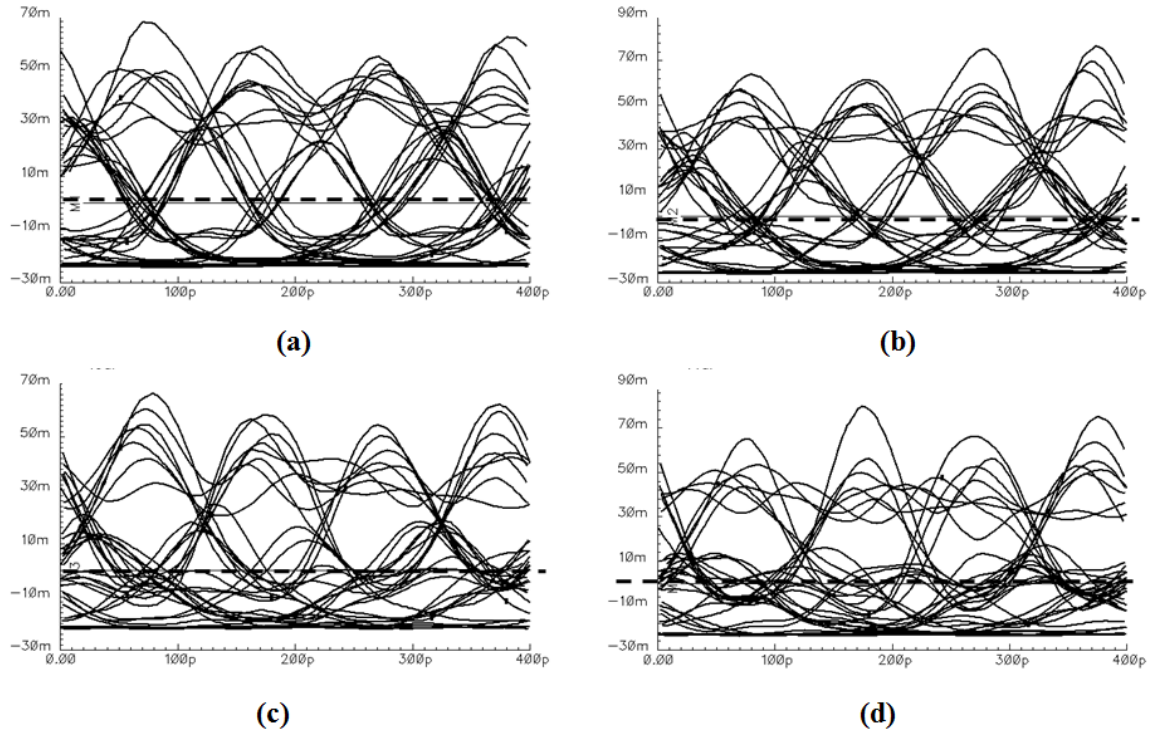


Figure 5.11 10-Gb/sec PRBS after (a) 80 km, (b) 100 km, (c) 120 km, (d) and 140 km of SMF [4.3].

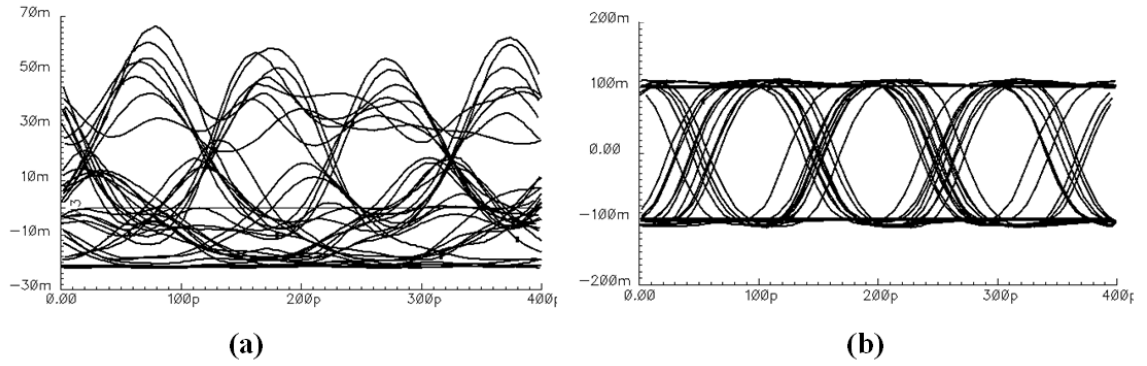


Figure 5.12 (a) After ADFE with I_{TAP} off and (b) After ADFE with I_{TAP} on [4.3].

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Technical Contributions

This work has developed and demonstrated a novel circuit architecture for decision-feedback equalization in order to overcome the first feedback-loop latency challenge of conventional DFEs operating at 10-Gb/sec. The work began with a study of pre-and post cursor ISI caused by bandwidth limitations in backplanes and dispersion in optical fibres. The DFE was identified as necessary for data recovery due to limitations in linear feed-forward equalizers. State-of-the-art DFE topologies were looked at and the dissertation illustrated how the clock-data delay of digital clocked comparators was the critical stumbling block in achieving a 10-Gb/sec DFE using the conventional topology.

The research showed that an ADFE was feasible by separating the data re-timing and equalization functions and performing decision-feedback equalization in the analog domain. The circuit building blocks for the ADFE were described and 10-Gb/sec equalization of FR-4 and MMF was shown. The main contributions of this work are:

1. A novel analog clock-less approach for decision-feedback equalization.
2. A 10-Gb/sec ADFE implemented in 0.18-um CMOS.
3. Successful equalization of up to 20 inches of FR-4 backplane at 10-Gb/sec
4. Successful dispersion compensation of 300 m MMF at 10-Gb/sec

5. Successful dispersion compensation of SMF up to 120 km at 10-Gb/sec.

6.2 Comparison with Published Literature

Table 6.1 summarizes other DFE circuits that have been published in the literature. To the author's knowledge, this work is the first to enable a 10-Gb/s DFE in a 0.18- μ m CMOS process. Other 10-Gb/sec DFE circuits are implemented in 90-nm CMOS. The continuous-time analog approach also consumes less power than comparable digital approaches. The ADFE with 2 forward taps and 2 feedback taps and output buffer consumes only 130 mW. A meaningful comparison with comparable digital structures would require a digital DFE with the same number of taps equalizing the same channels and monitoring power consumption and output BER. Most DFEs in the literature are part of a larger circuit including CDR and digital circuitry and so a symmetric comparison is not possible. However, the numbers in the table give an idea of the savings in power with the analog DFE approach. The circuit described in [6.1] is a 10-Gb/sec DFE that is used to equalize a 20-inch FR-4 channel. This DFE consists of a 4-tap FFE and a 5-tap DFE and consumes at least 600 mW of power. Although this is not a symmetric comparison because of the reasons stated above, it gives an idea to the savings in power that can be achieved with an unclocked approach. Figure 6.1 plots the trend of published DFE circuits. The operating speed is plotted against the process technology used. As expected, increased operating speeds necessitate a move to smaller CMOS process nodes. The published DFES sit on the curve. The ADFE shown in this work is to the left of the trend curve. This means that scaling the design to smaller nodes can achieve higher data rates.

An ADFE implemented in 90-nm CMOS could be designed to operate at data rates 20-Gb/sec or higher.

Table 6.1 Comparison with published literature.

Source	Data rate (Gb/sec)	Features	CMOS Tech.	Topology	Power
TI [3.3]	6.25	4FFT/4FBT	0.13- μ m	$\frac{1}{2}$ -rate clocking	7W
Synopsys [2.13]	6.25-9.6	1FFT/1FBT	0.13- μ m	Unrolled first tap + $\frac{1}{2}$ -rate clocking	152mW
LSI Logic [3.1]	6.4	2FFT/4FBT	0.13- μ m	Pre-calculation + $\frac{1}{4}$ -rate clocking	~310mW
IBM [6.1]	10	4FFT/5FBT	90-nm	First tap speculation	> 600mW
This work	10	4FFT/1FBT	0.18- μ m	ADFE	352mW
This work	10	2FFT/2FBT		ADFE	130mW

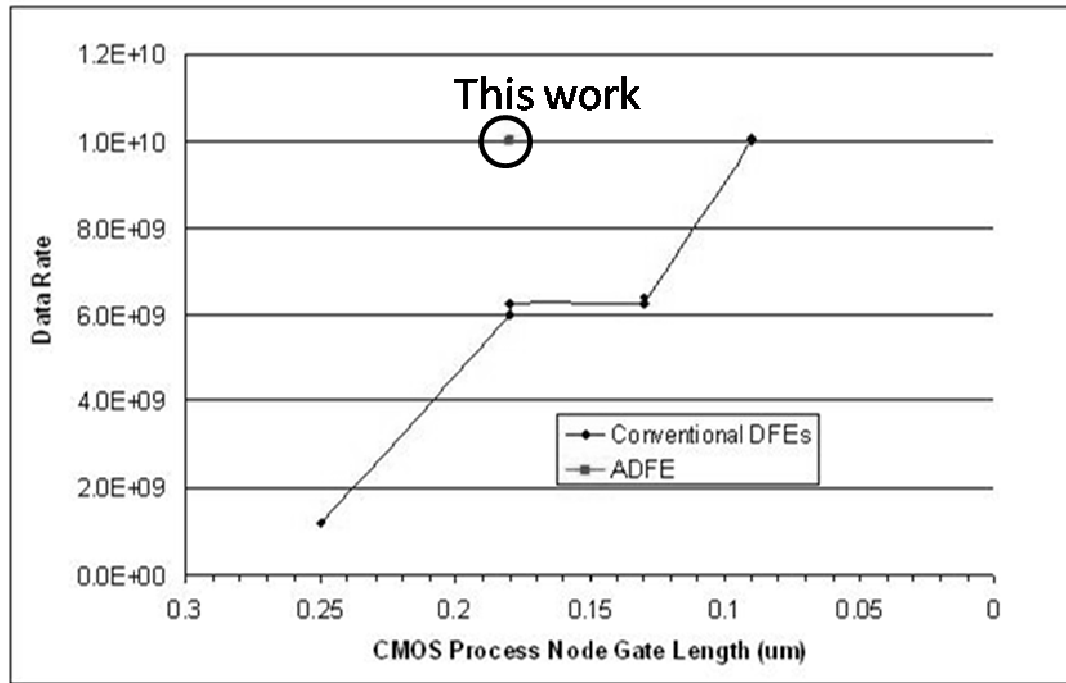


Figure 6.1 Published DFE operating speeds vs. process node.

6.3 Future Directions

The output of the ADFE suffers from significant jitter when fed with a signal with a closed eye-diagram. The input is impaired with jitter to begin with and although the output eye is open at the centre, the edges suffer from jitter. Future work would involve timing the output data at the centre of the output eye with a recovered system clock in order to improve the jitter performance.

One of the important results of this work is that 10-Gb/sec decision feedback was shown in a 0.18-um CMOS process. This means that if the ADFE was scaled to smaller process nodes, much faster data rates could be obtained. Future work could be aimed at 20-Gb/sec to 40-Gb/sec DFEs for optical receiver applications.

The purpose of this work was to demonstrate a novel analog technique and circuit architecture to achieve the benefits of decision-feedback equalization in a standard CMOS process for equalization of bandwidth and dispersion limited legacy channels at 10-Gb/sec. As such, the primary focus of this work was on the high-speed signal path. The low-speed control voltages are tuned manually during testing. In order for the circuit to be fully functional in a product environment, the ADFE must automatically adapt to changes in channel. This would involve the design of an adaptation loop that would sample the input and output of the ADFE and update the tap coefficients and delay control voltages automatically using the MMSE or LMS algorithm. Future work could focus on the design of the control loop for the ADFE in order to achieve a complete adaptive receiver equalizer solution that can be used for a variety of channels.

Feedback loop stability might be an issue as we increase the number of feedback taps. The feedback is essentially non-linear. Therefore, traditional linear gain and phase stability analysis using Bode plots does not apply. The ADFE has shown stable operation up to 2 feedback loops. Increasing the number of feedback taps beyond two may result in instabilities. Future work can involve investigation of multiple feedback loop stability.

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